

NOTE: THIS Dwg. S/B
ENHANCED, AS PER,
EG. 6, 055, 295

RADIATION GENERATION
SYSTEM

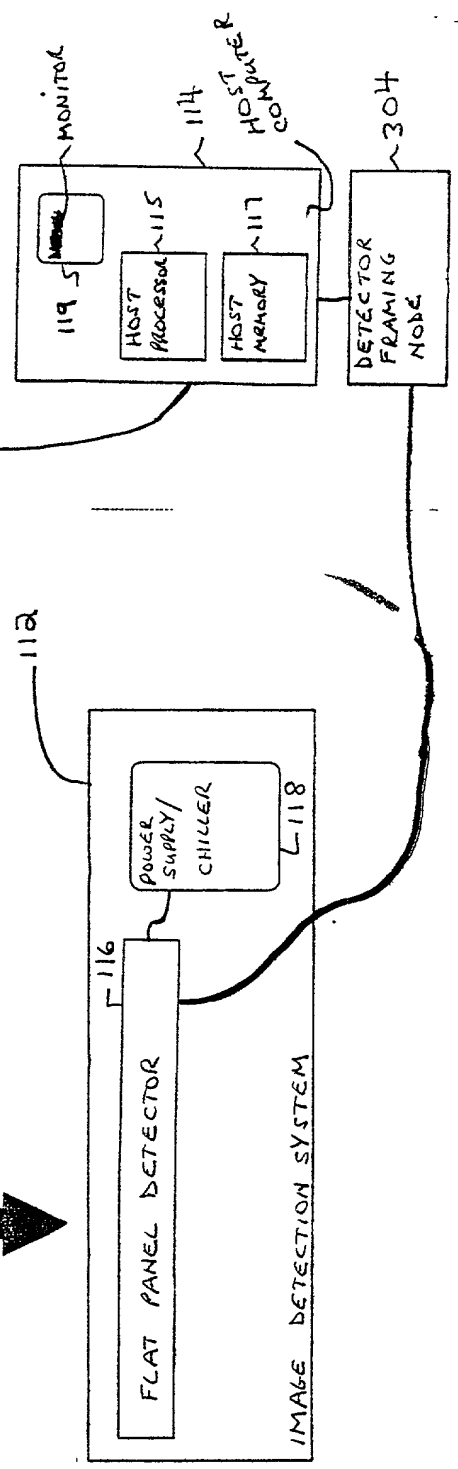
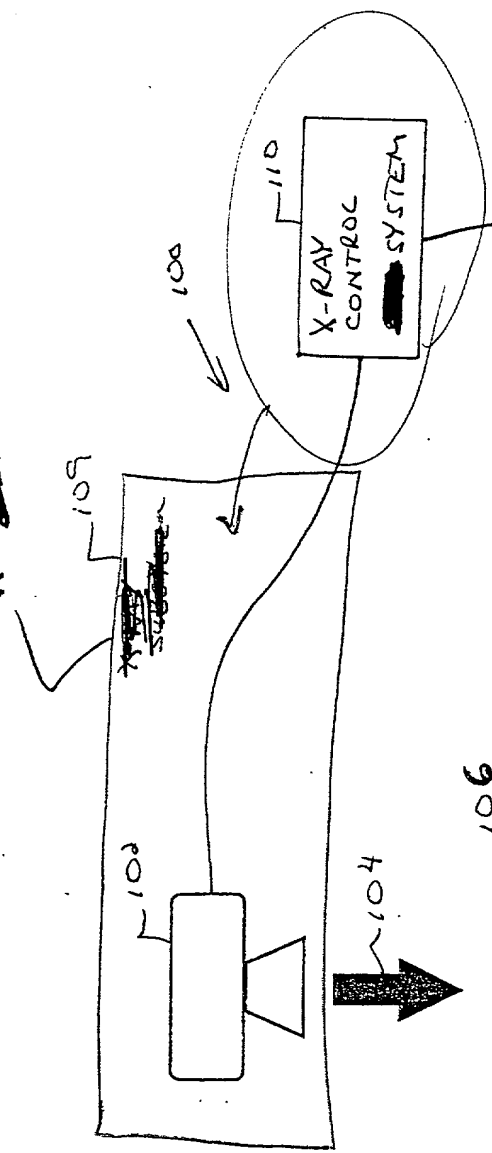


FIG. 1

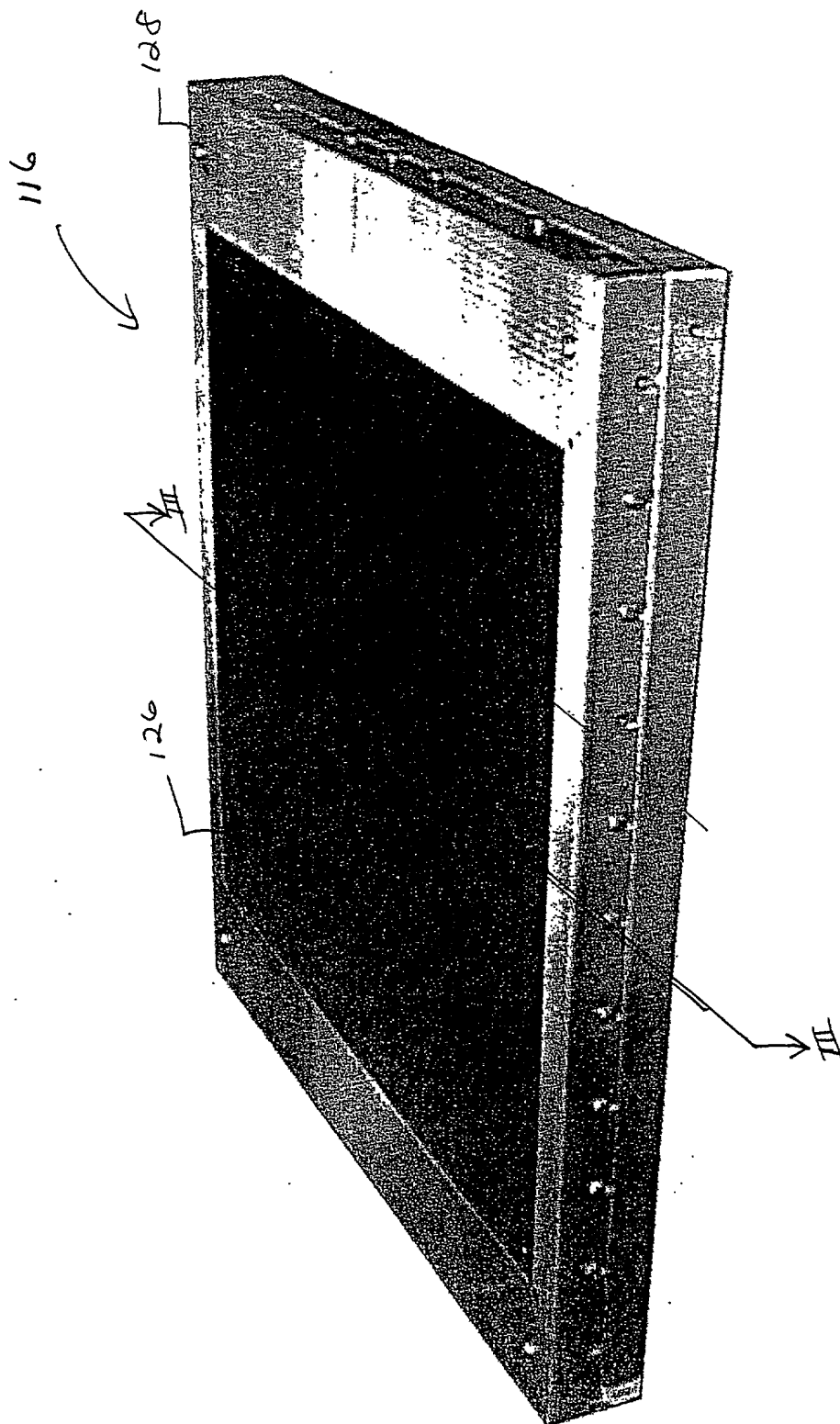


FIG. 2 (PRIOR ART)

116 128 130 132 134 136 138 140 142 144

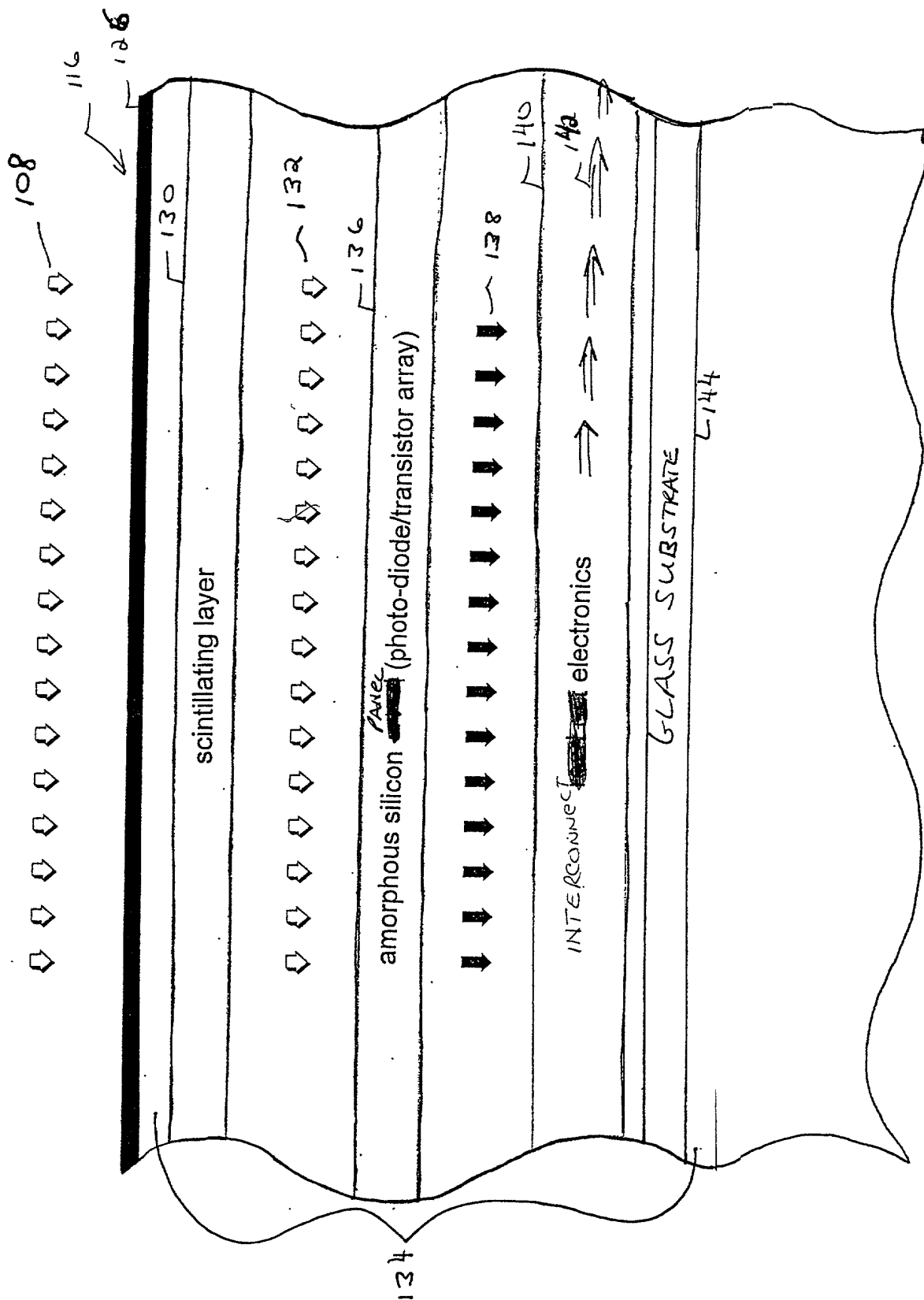


FIG. 3

FIG. 4 is a perspective view of a prior art device, showing a curved surface 134, a grid-like structure 136, a curved surface 144, a curved surface 146, a curved surface 150, a curved surface 148, and a curved surface 130.

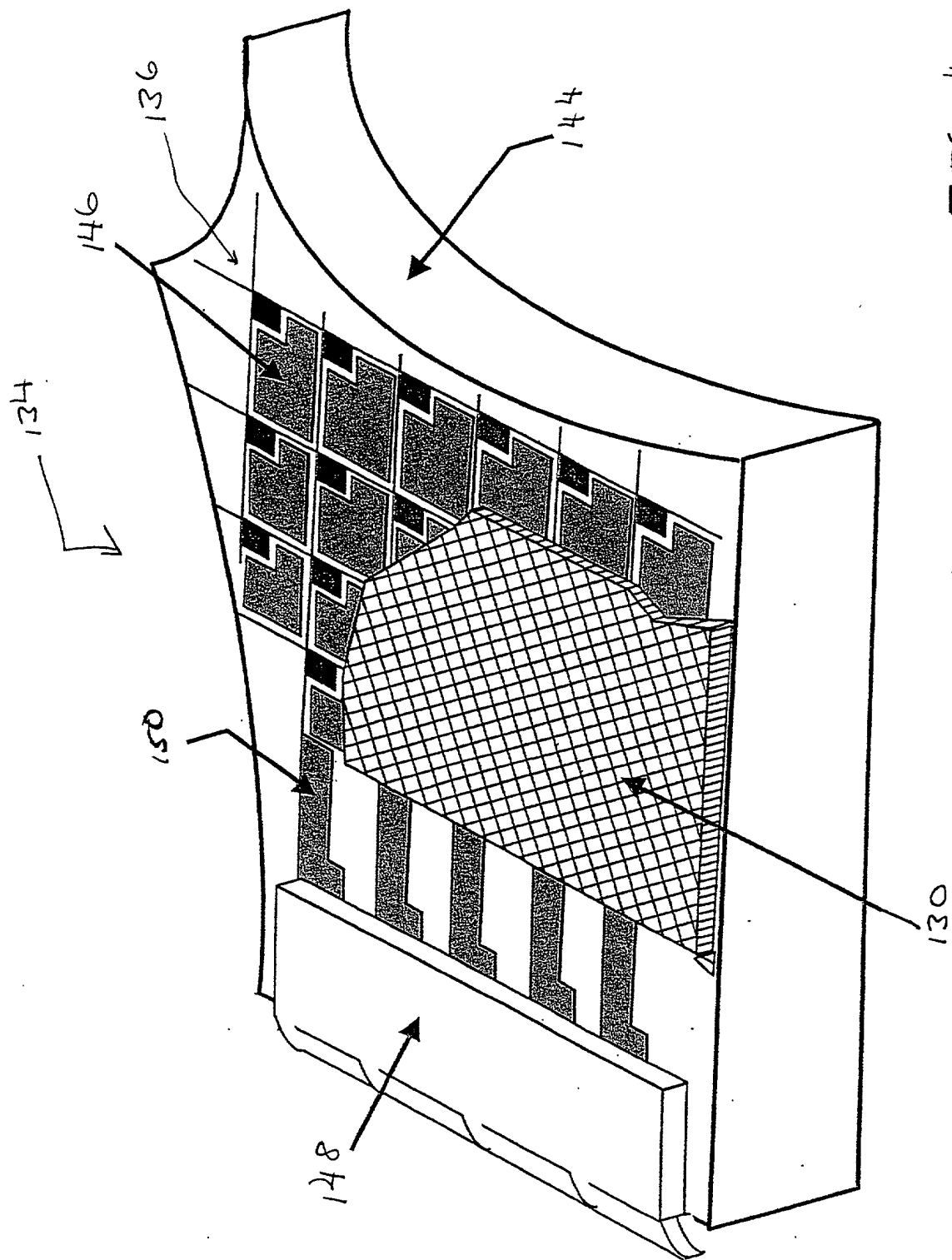


FIG. 4
(PRIOR ART)

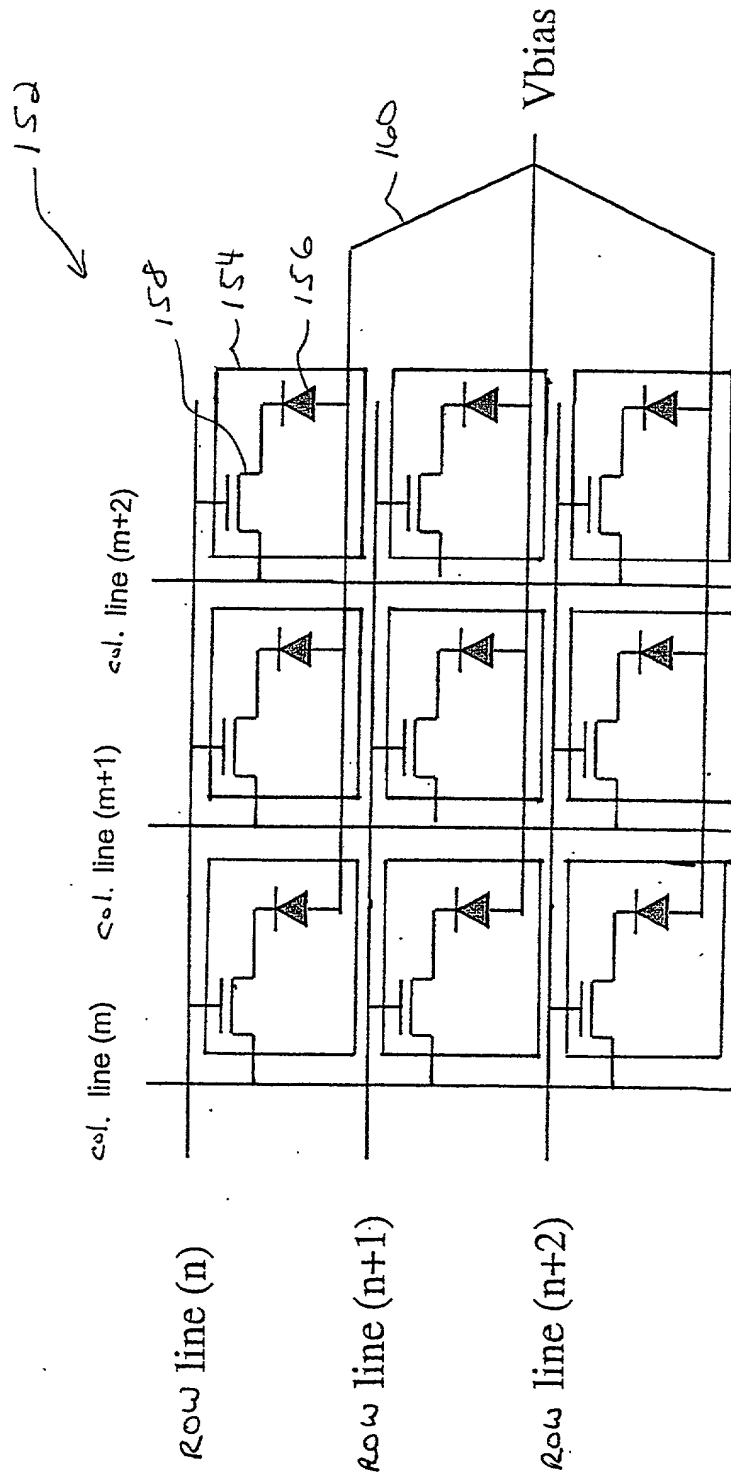


FIG. 5
(Prior Art)

FLAT PANEL DETECTOR

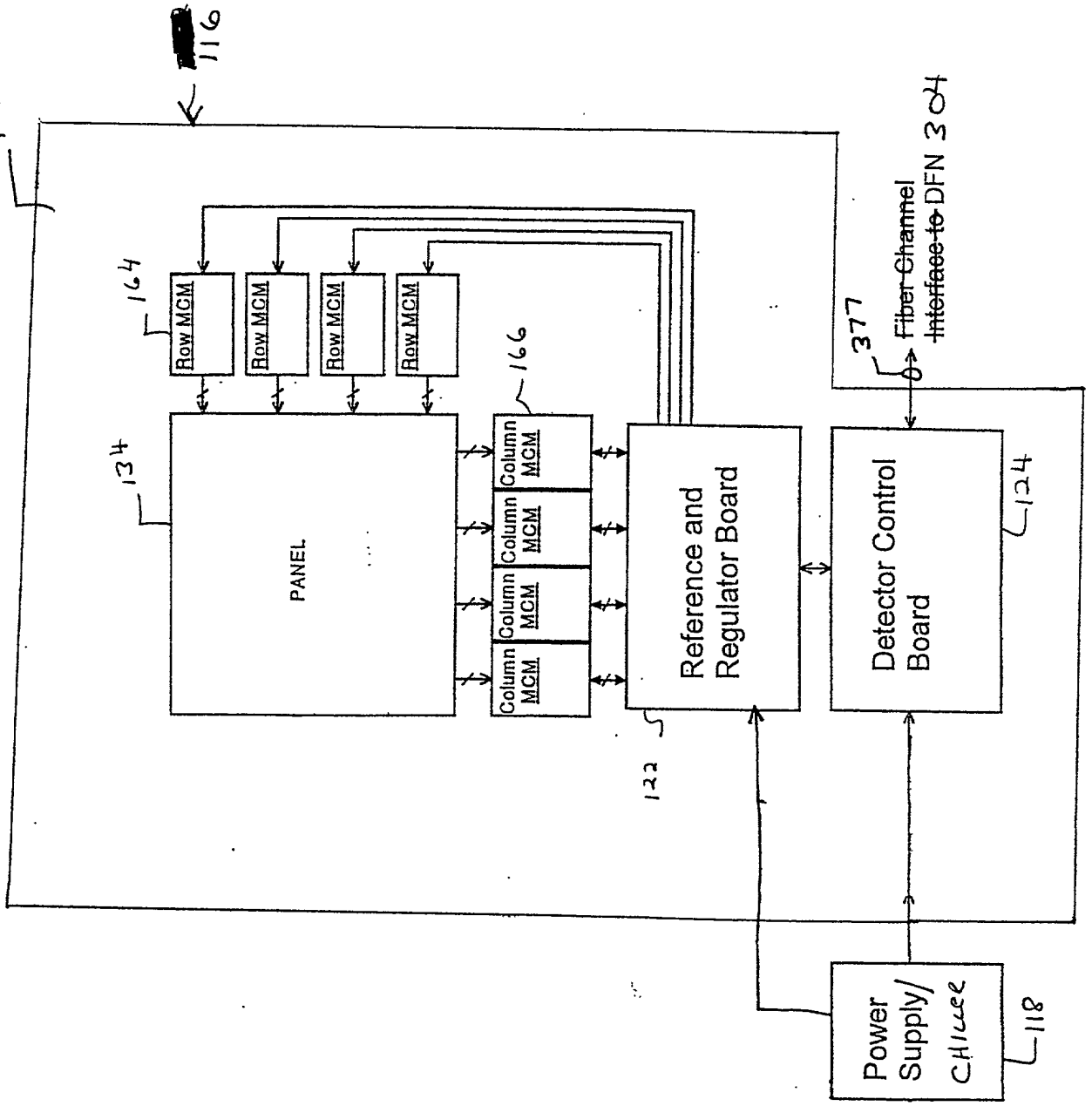


FIG. 6
(PRIOR ART)

FLAT PANEL DETECTOR

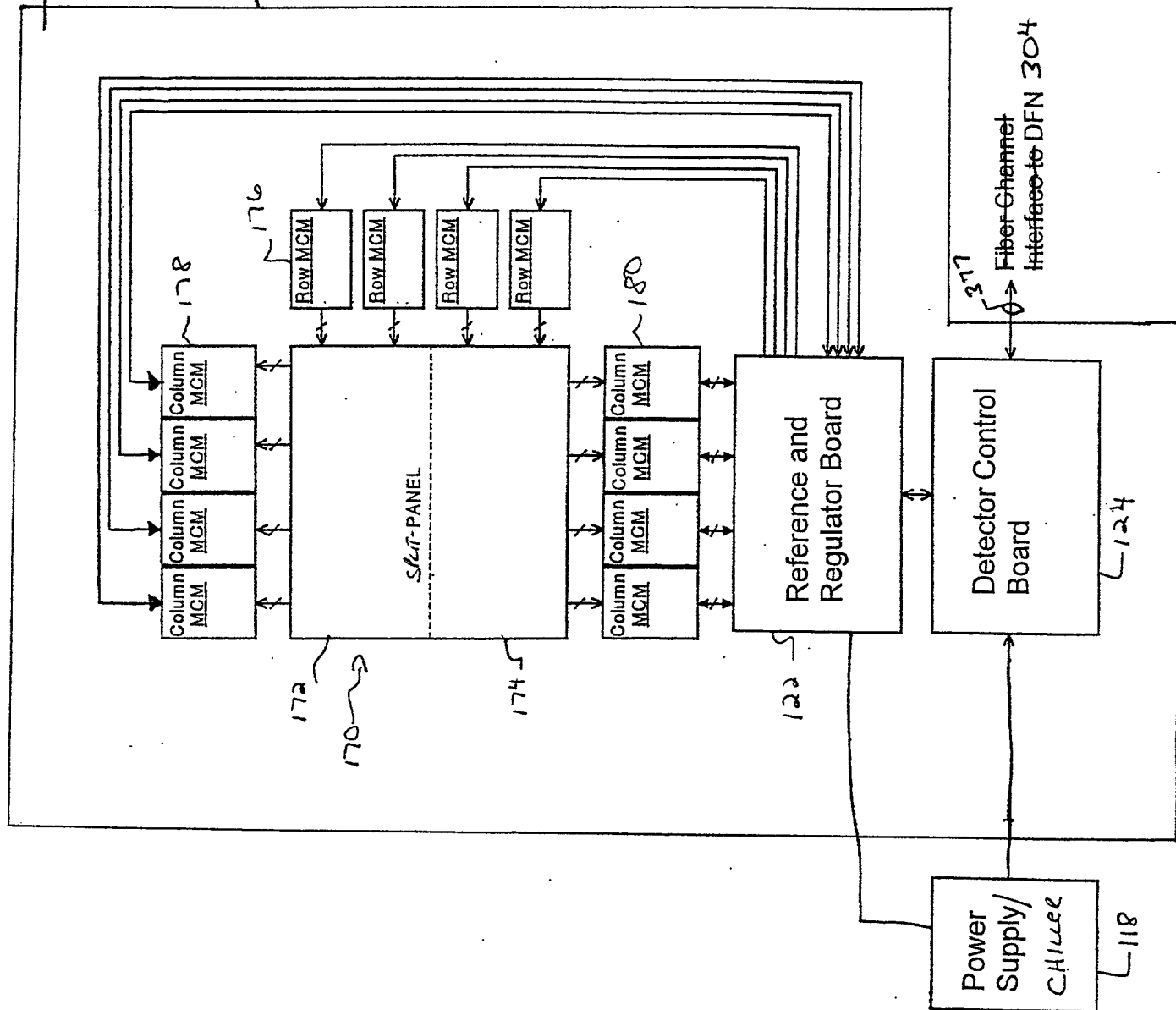
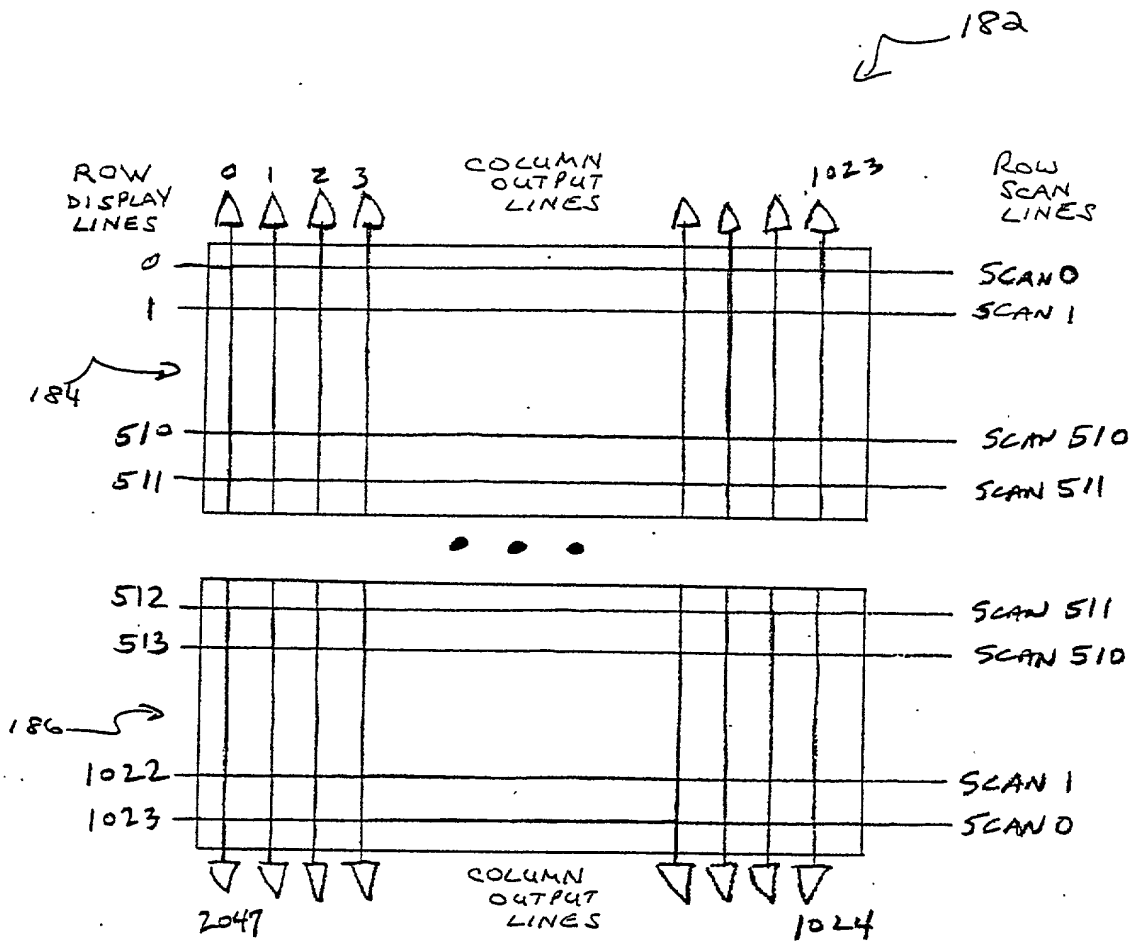


FIG. 7
(PRIOR ART)



CARDIAC/SURGICAL DIGITAL X-RAY PANEL

FIG. 8
(PRIOR ART)

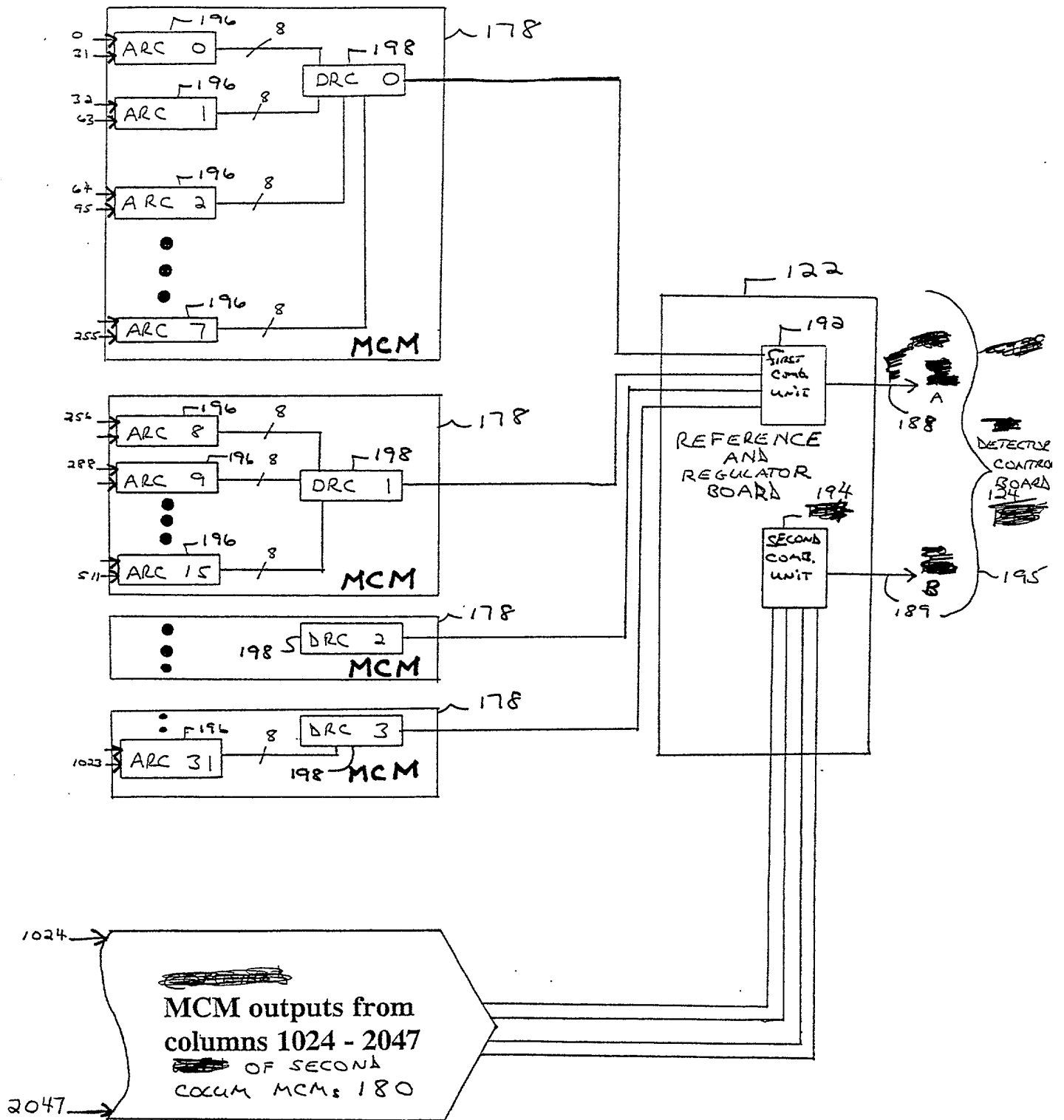


FIG. 9
(PRIOR ART)

FIG. 10 is a block diagram of a detector control board, showing the internal components and their interconnections. The board is divided into several functional blocks, including an F.O. Transceiver, F.O. Detector, Encoder/Decoder Unit, and a Control Unit. The diagram illustrates the flow of data and control signals between these components, as well as the board's connections to an Image Detection Bus and a Reference and Register Board.

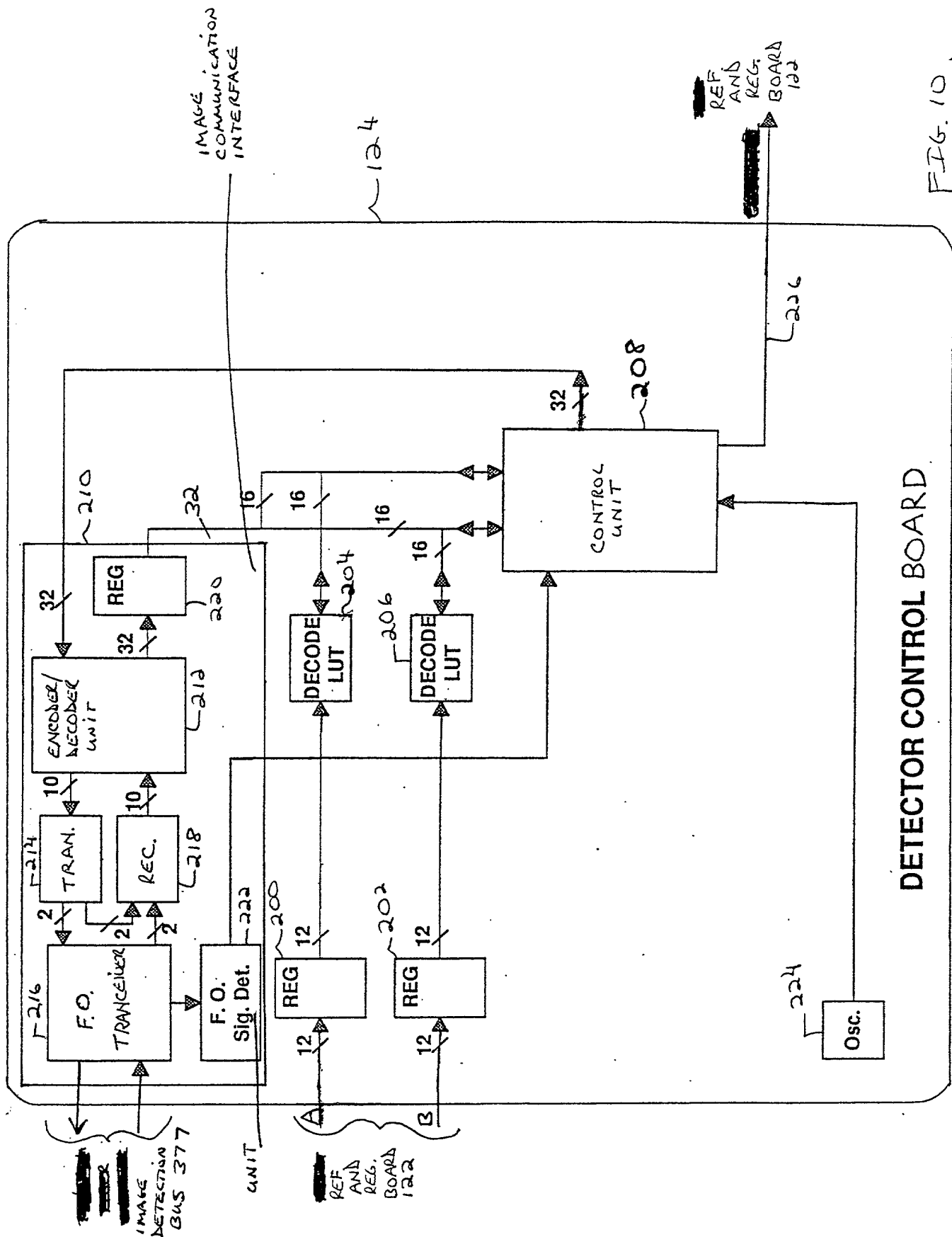
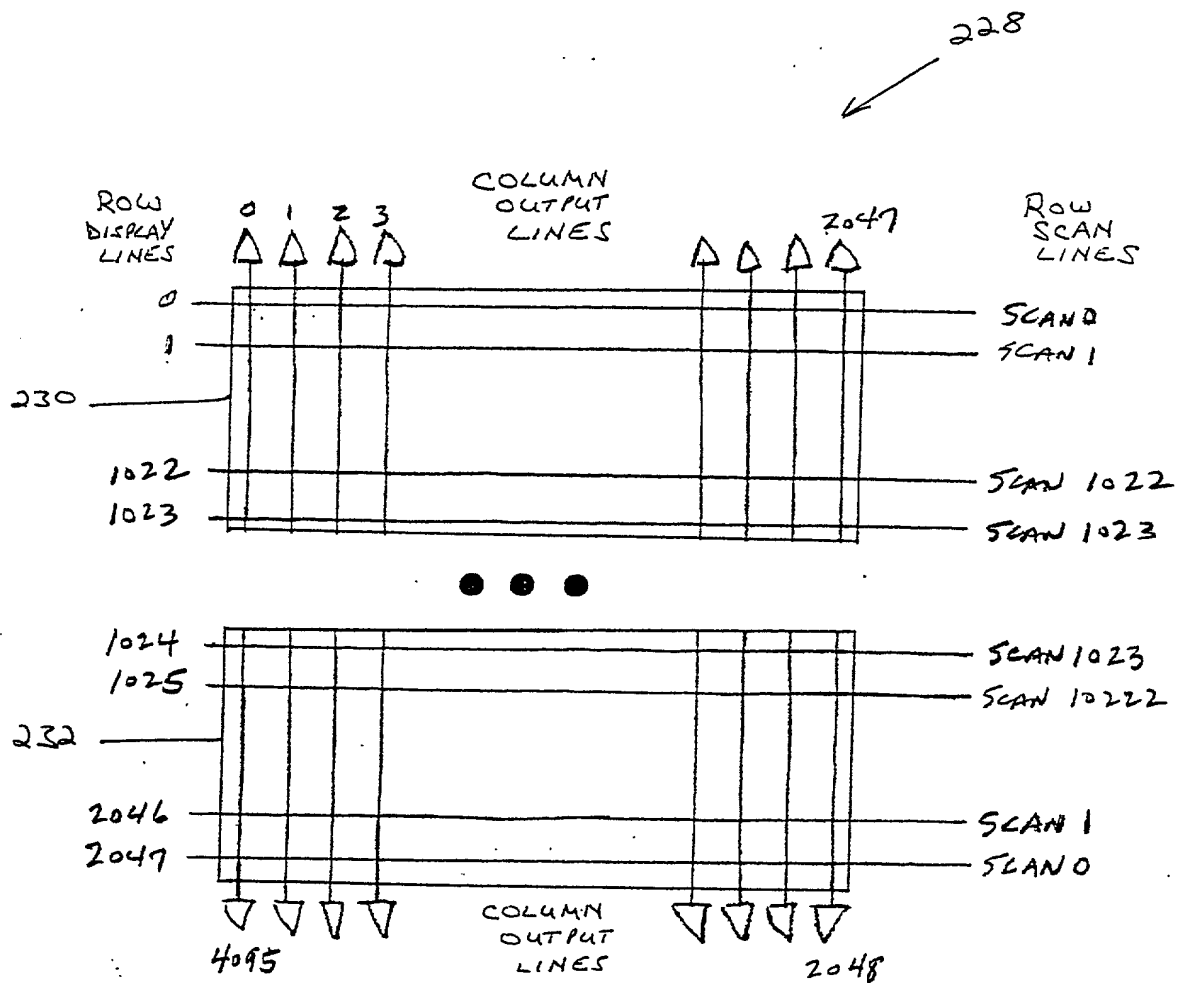


FIG. 10
(PRIOR ART)



RADIOGRAPHY DIGITAL X-RAY PANEL

FIG. 11
(PRIOR ART)

FIG. 12 is a block diagram of a flat panel detector system. The system includes a flat panel detector 116, a reference and regulator board 122, a detector control board 124, a power supply/chiller 118, and a fiber channel interface to DFN 304. The flat panel detector 116 is connected to the reference and regulator board 122 via a bus 236. The reference and regulator board 122 is connected to the detector control board 124 via a bus 124. The detector control board 124 is connected to the fiber channel interface to DFN 304 via a fiber channel interface 317. The power supply/chiller 118 provides power to the reference and regulator board 122 and the detector control board 124.

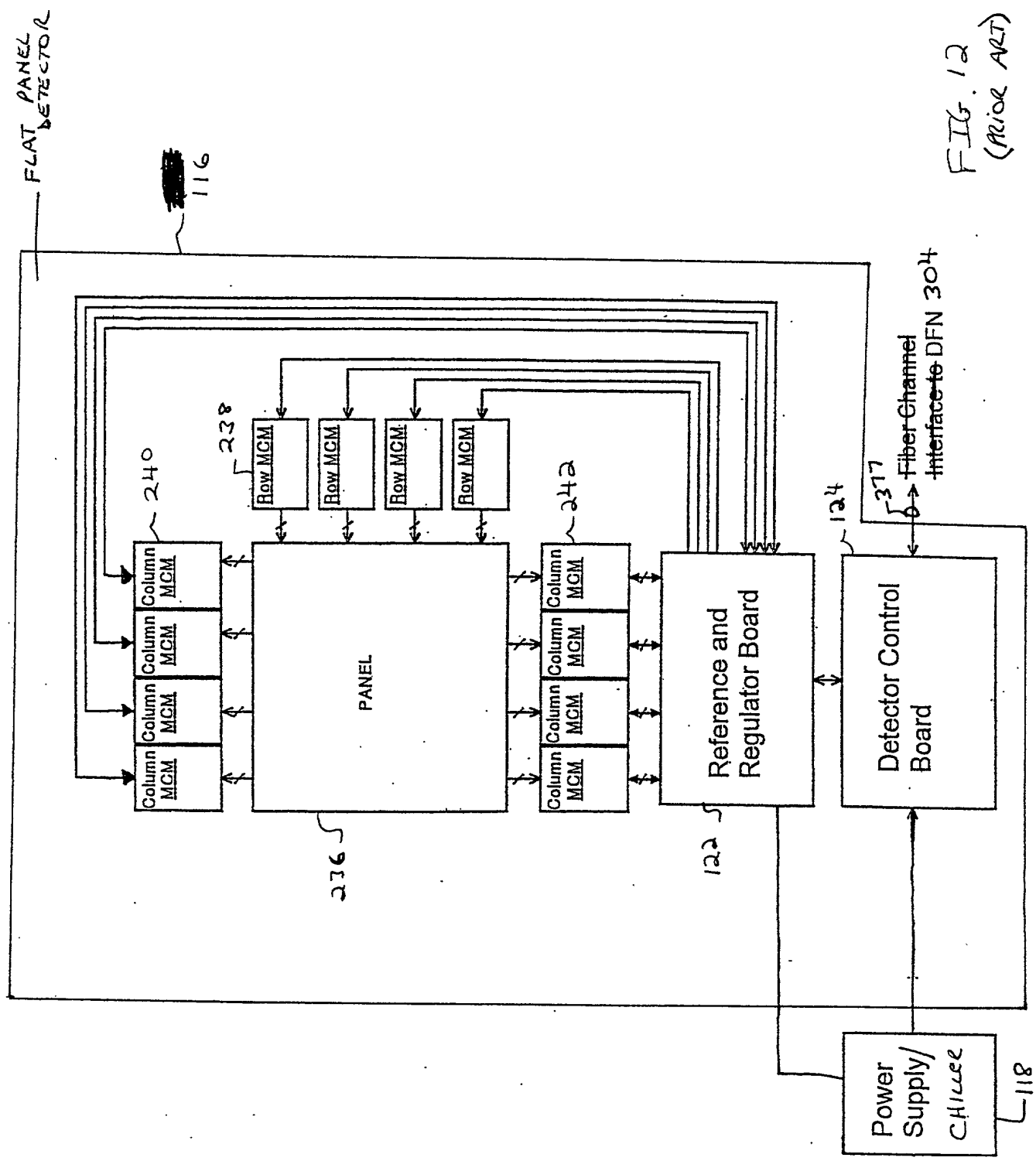
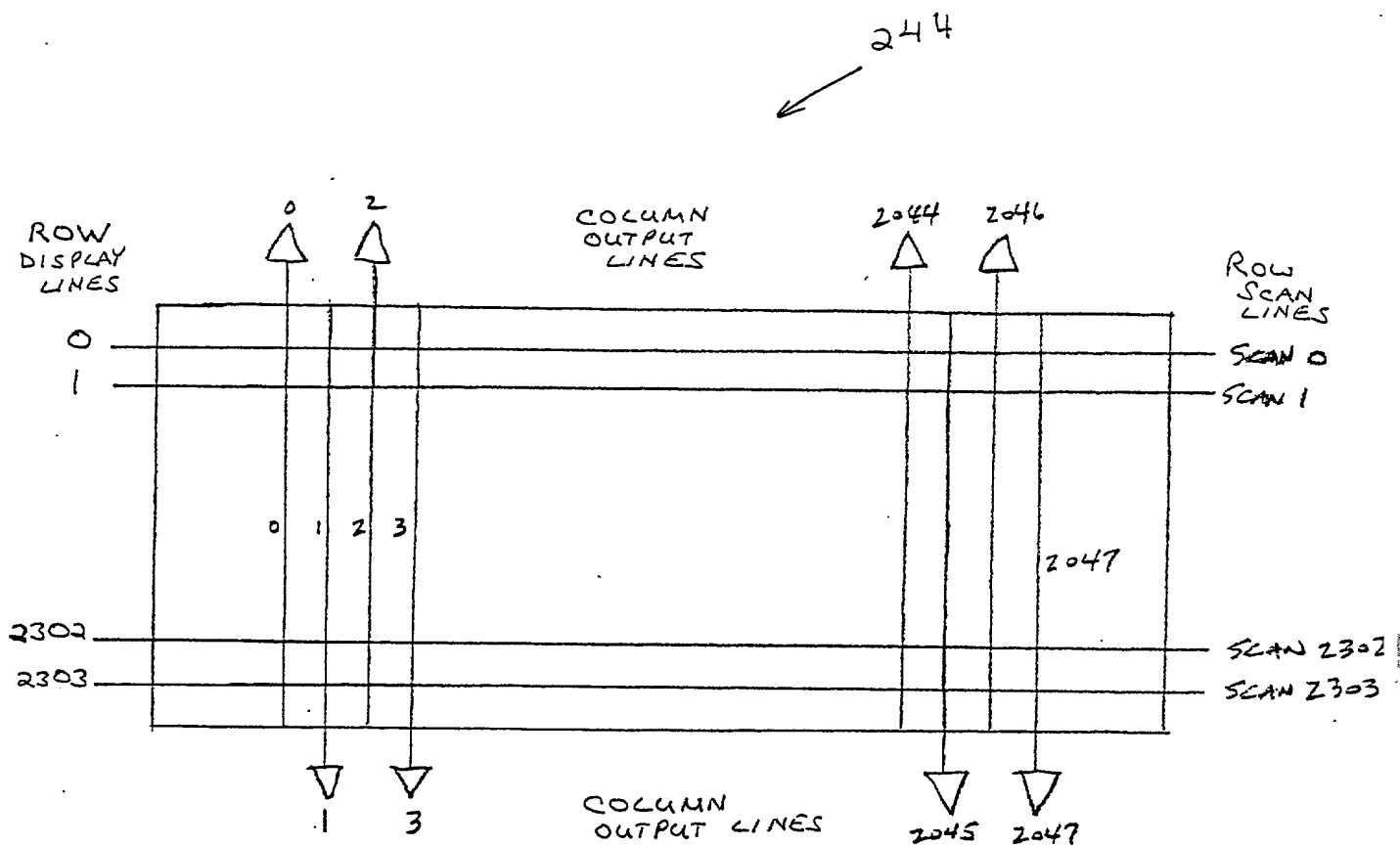


FIG. 12
(Prior Art)

and that the time off of the beam is
time and that it is then that the beam



MAMOGRAPHY DIGITAL X-RAY PANEL

FIG. 13
(PRIOR ART)

FLAT PANEL
DETECTOR

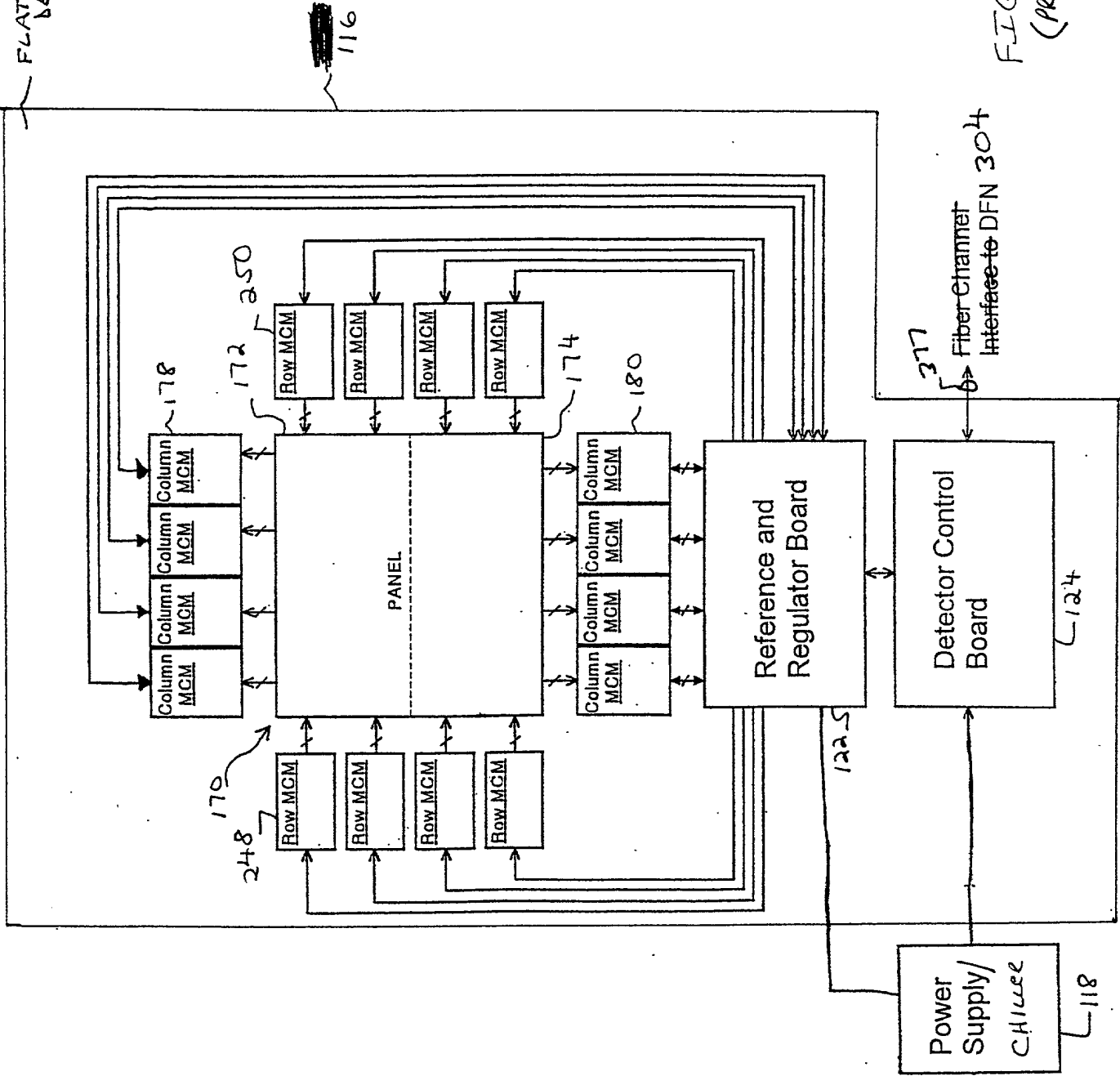
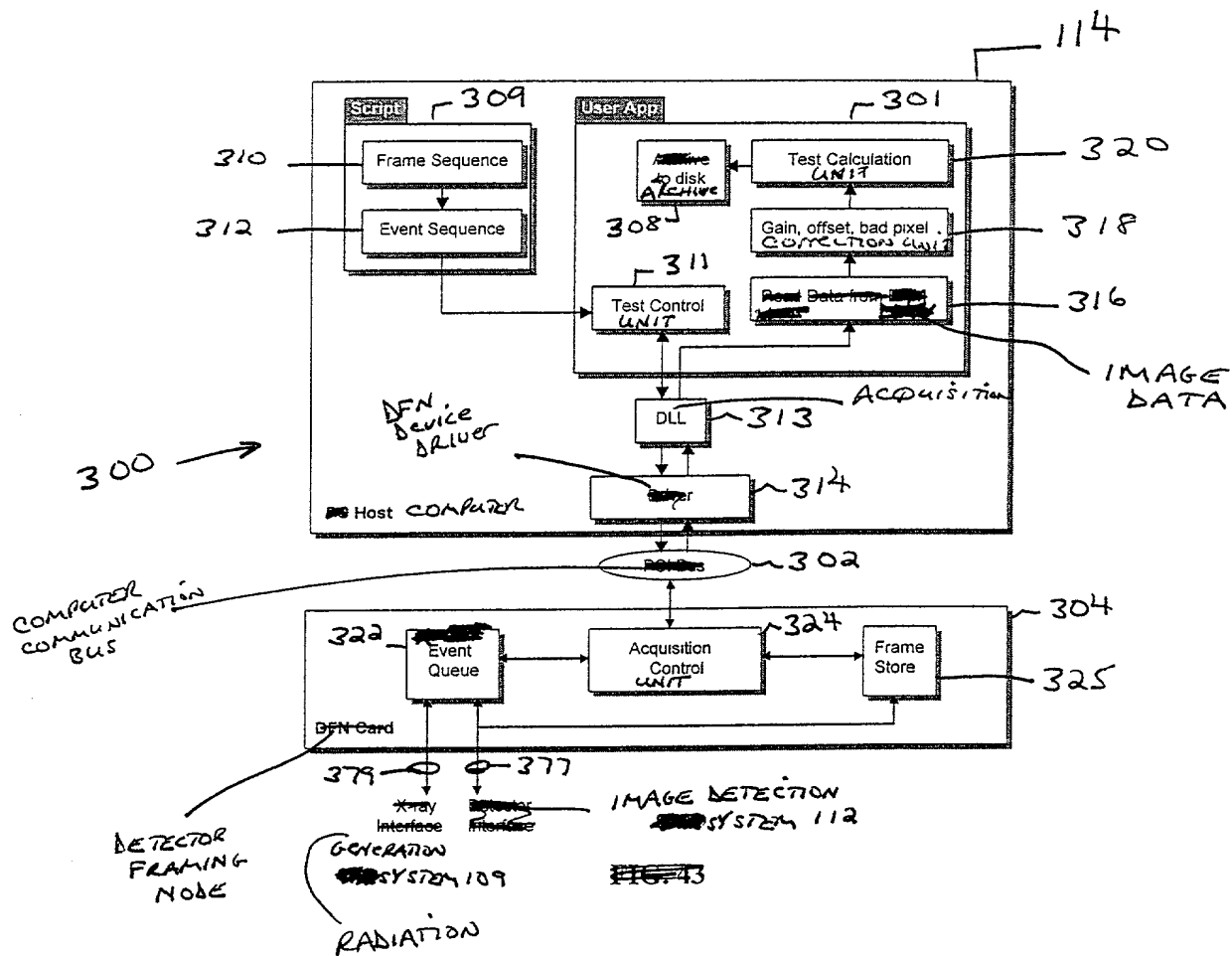
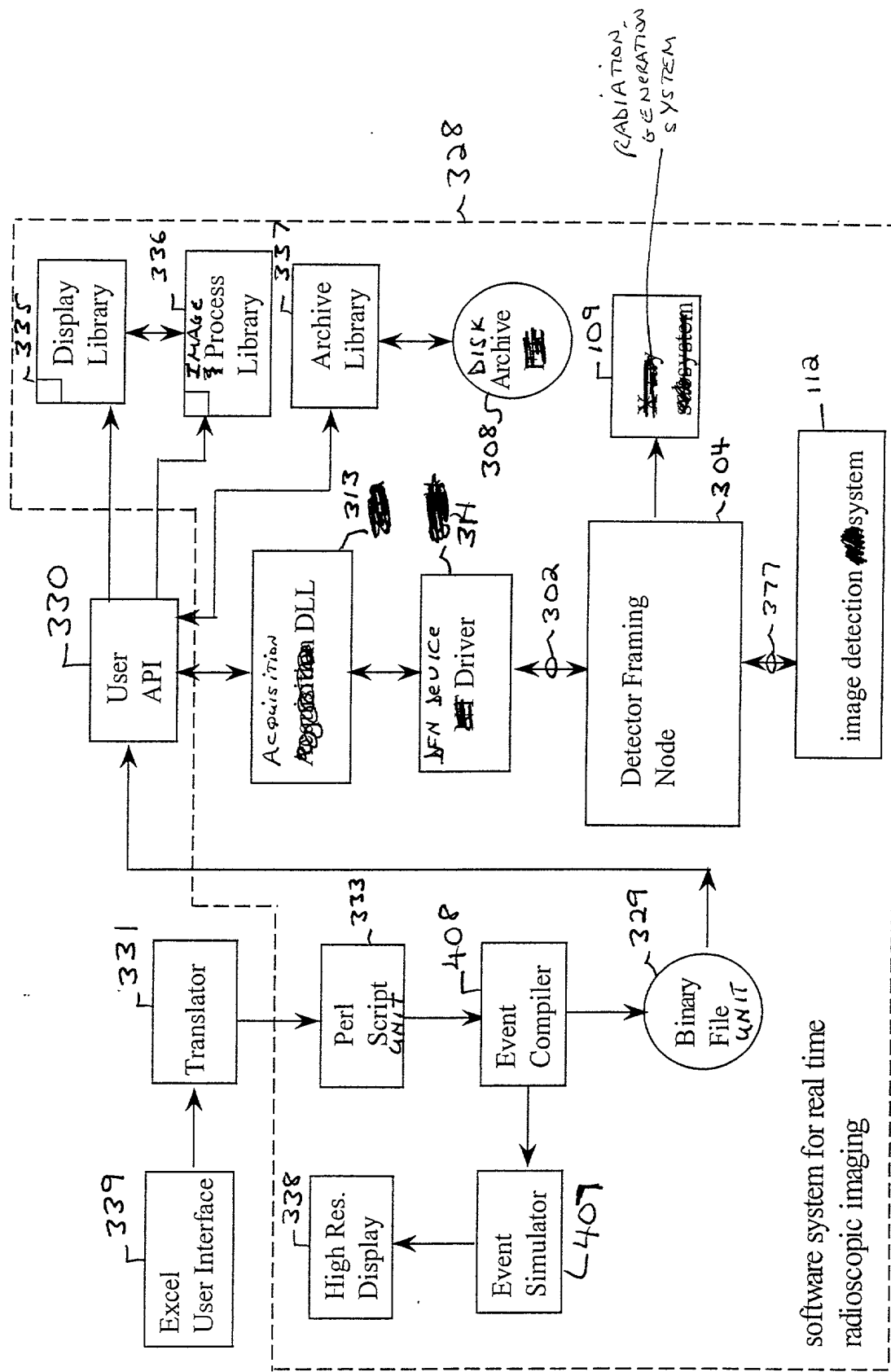


FIG. 14
(Prior Art)



w:\1346\todd-dfn cases\drawings\dwg-01 (page 3)



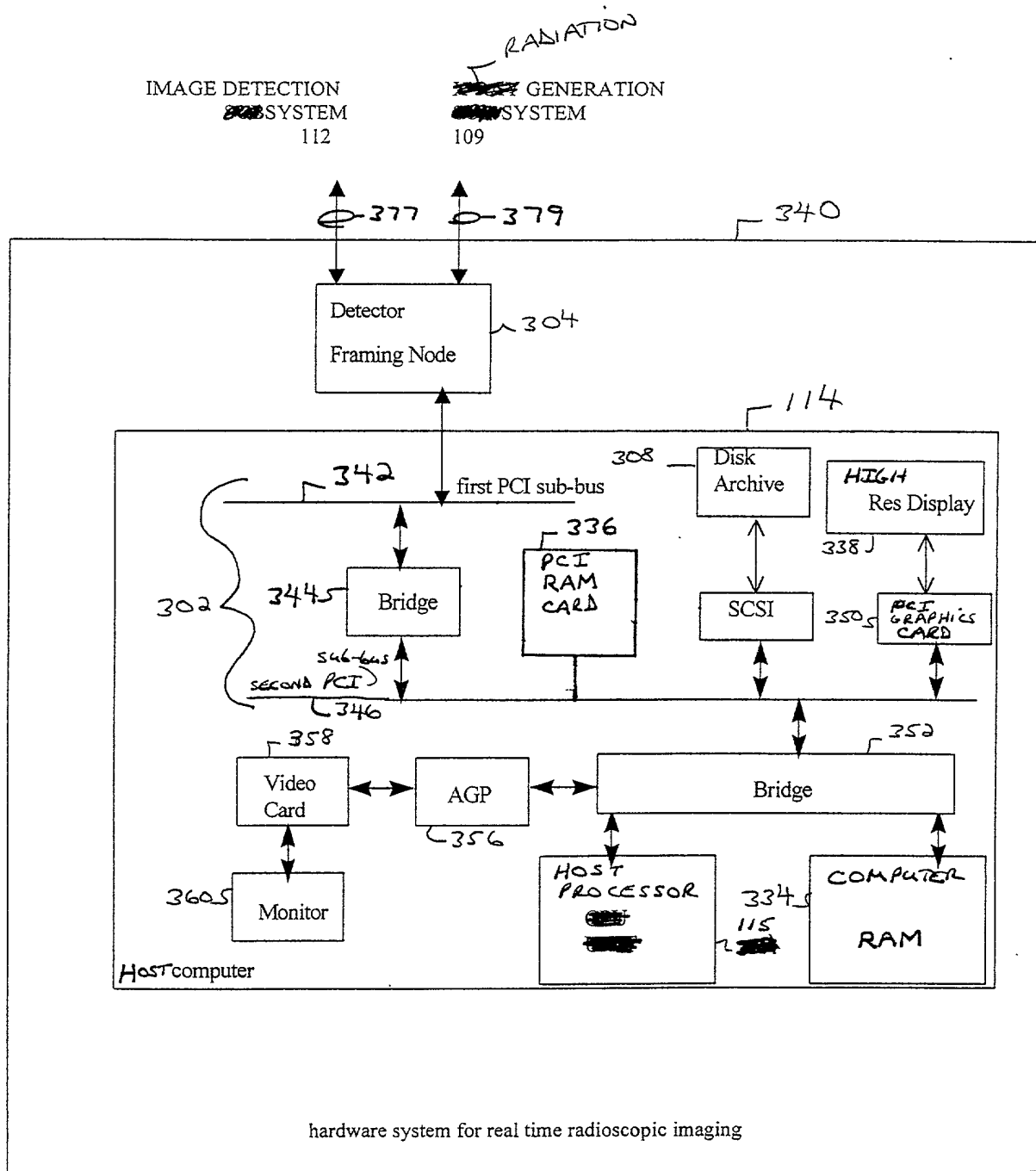


FIG. 17

13

FRAME BUFFER MEMORY

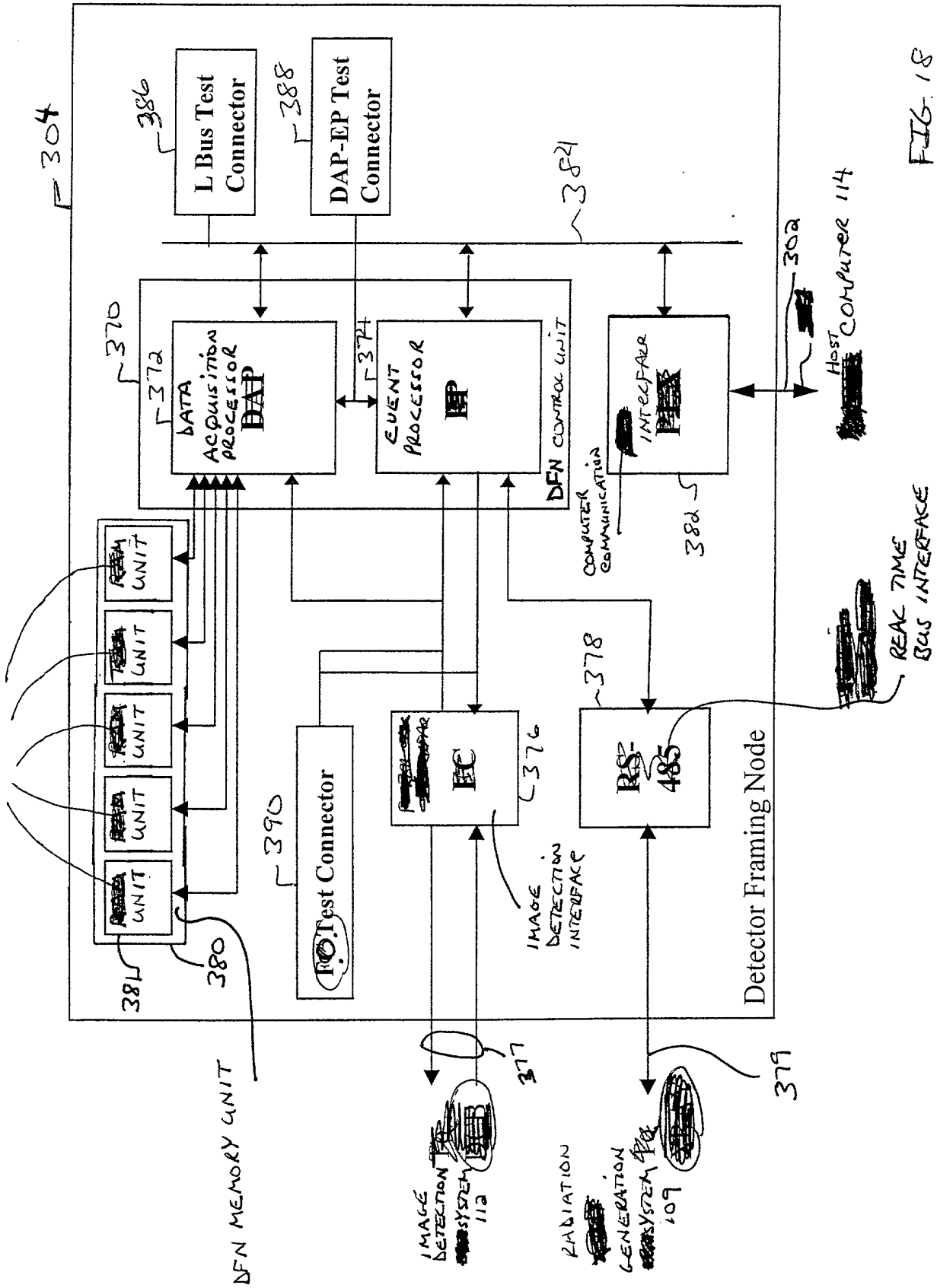


FIG. 18

W:\1346\todd-DFN cases\drawings\estimated image processing.doc

W:\1346\todd-DFN cases\drawings\estimated image processing.doc

Panel Setup	Real Time	(fm/sec)	length	Latency	memory	offset	gbr
Single Frame	Post Process	30	unlimited	< 5 frames	host	none	
Single Frame	Post Process	-	-	Delay ~.1 sec	"	y	
		-	-	Delay ~.2 sec	"	y	y
Real Time	Real Time	R	Unlimited	< 5 frames	host	none	
Real Time	Real Time	R - X	Unlimited	< 5 frames	"	y	
Real Time	Real Time	R - Y	Unlimited	< 5 frames	"	y	y

FIG-19

Modality	image size	Frames Stored
Cardiac	1024 x 1024	host memory
Rad	2048 x 2048	200
Mammo	2304 x 2048	50
		44

FIG. 20

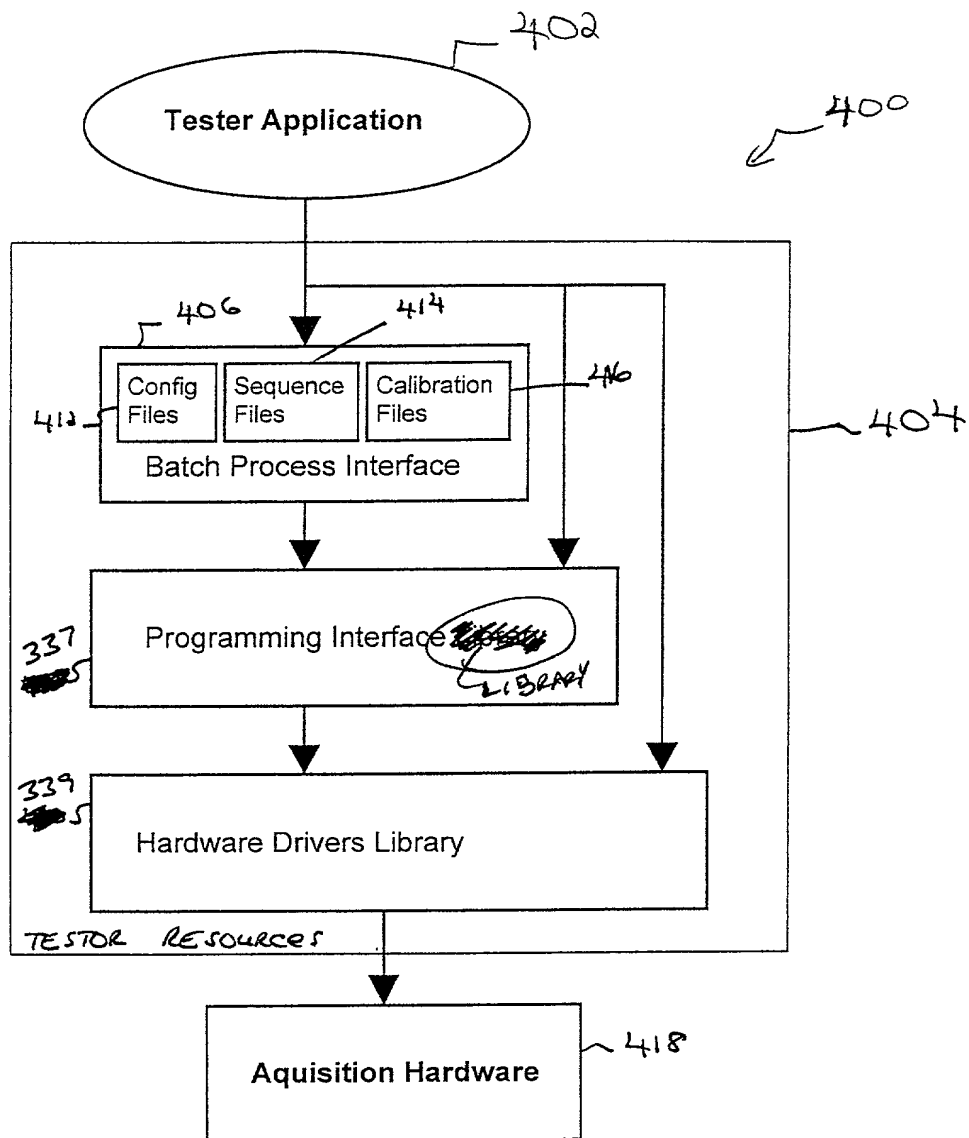


FIG. 21

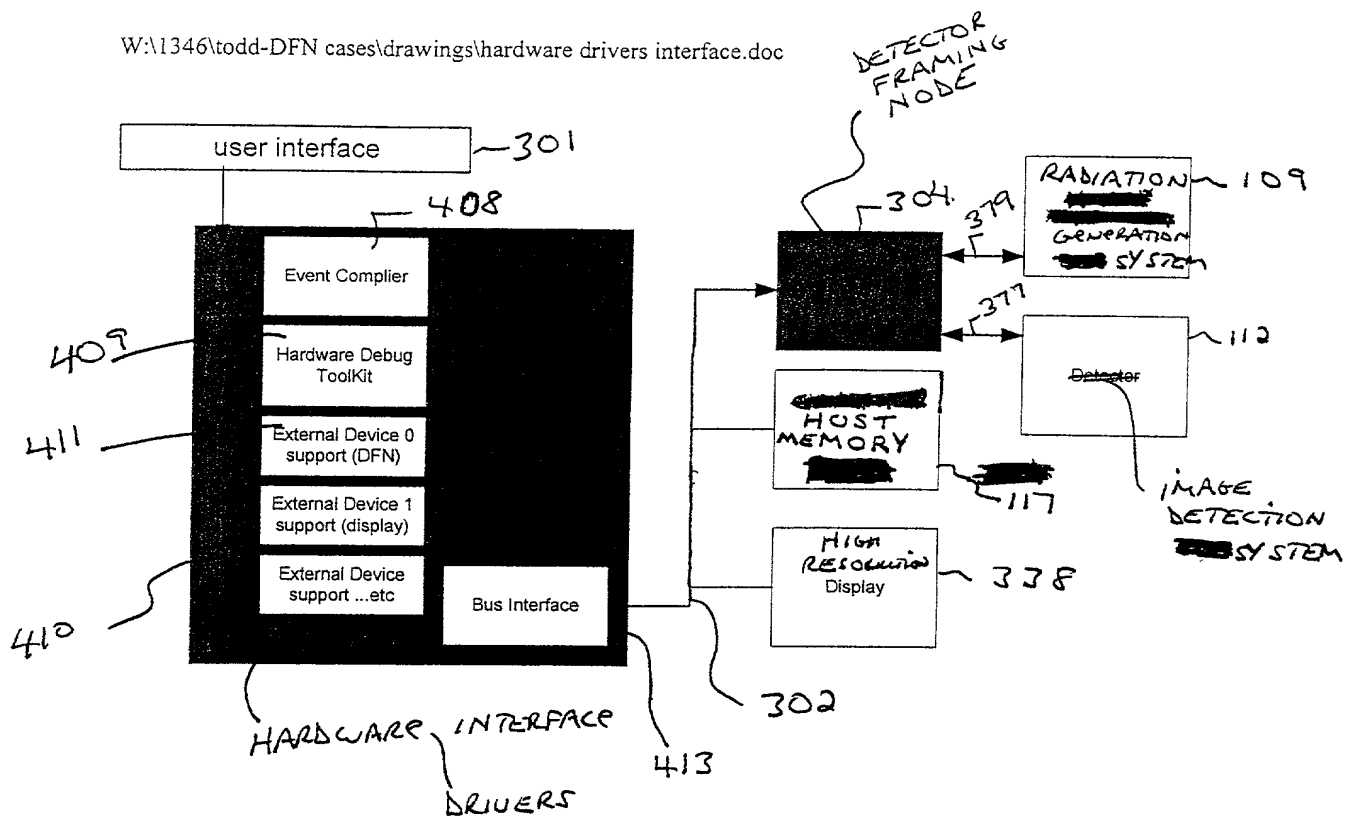


FIG. 22

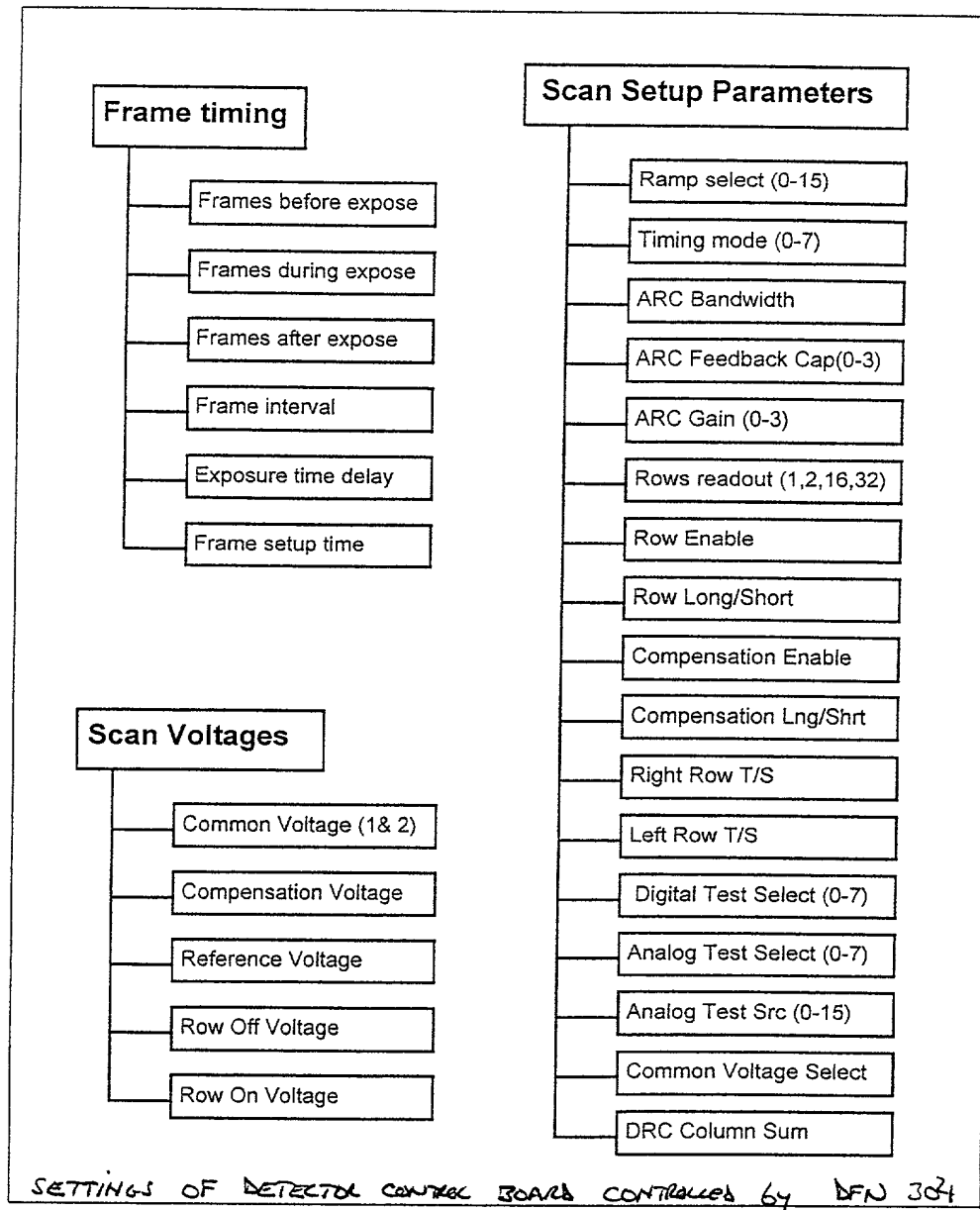


FIG. 23

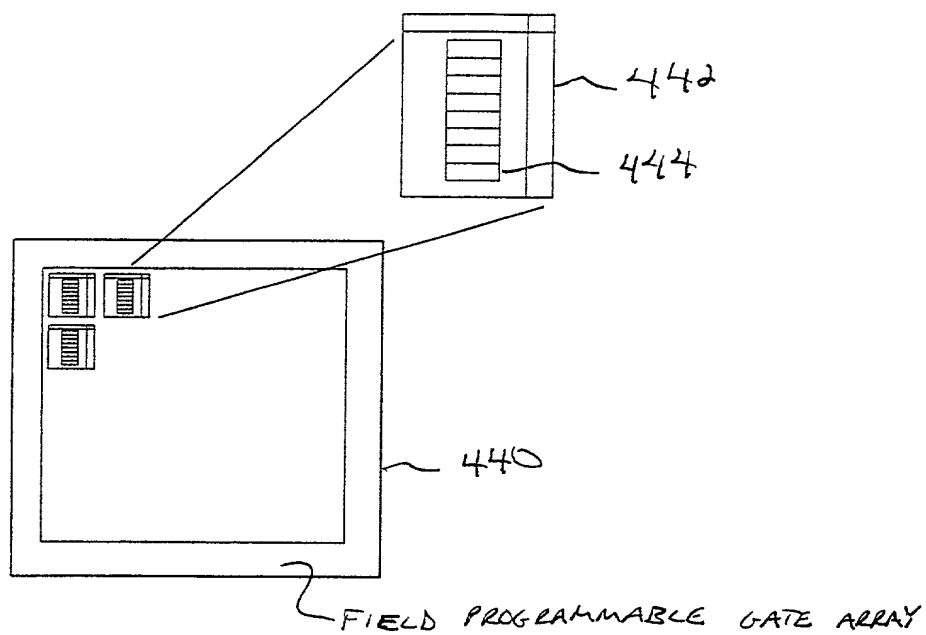


FIG. ~~23~~ 24

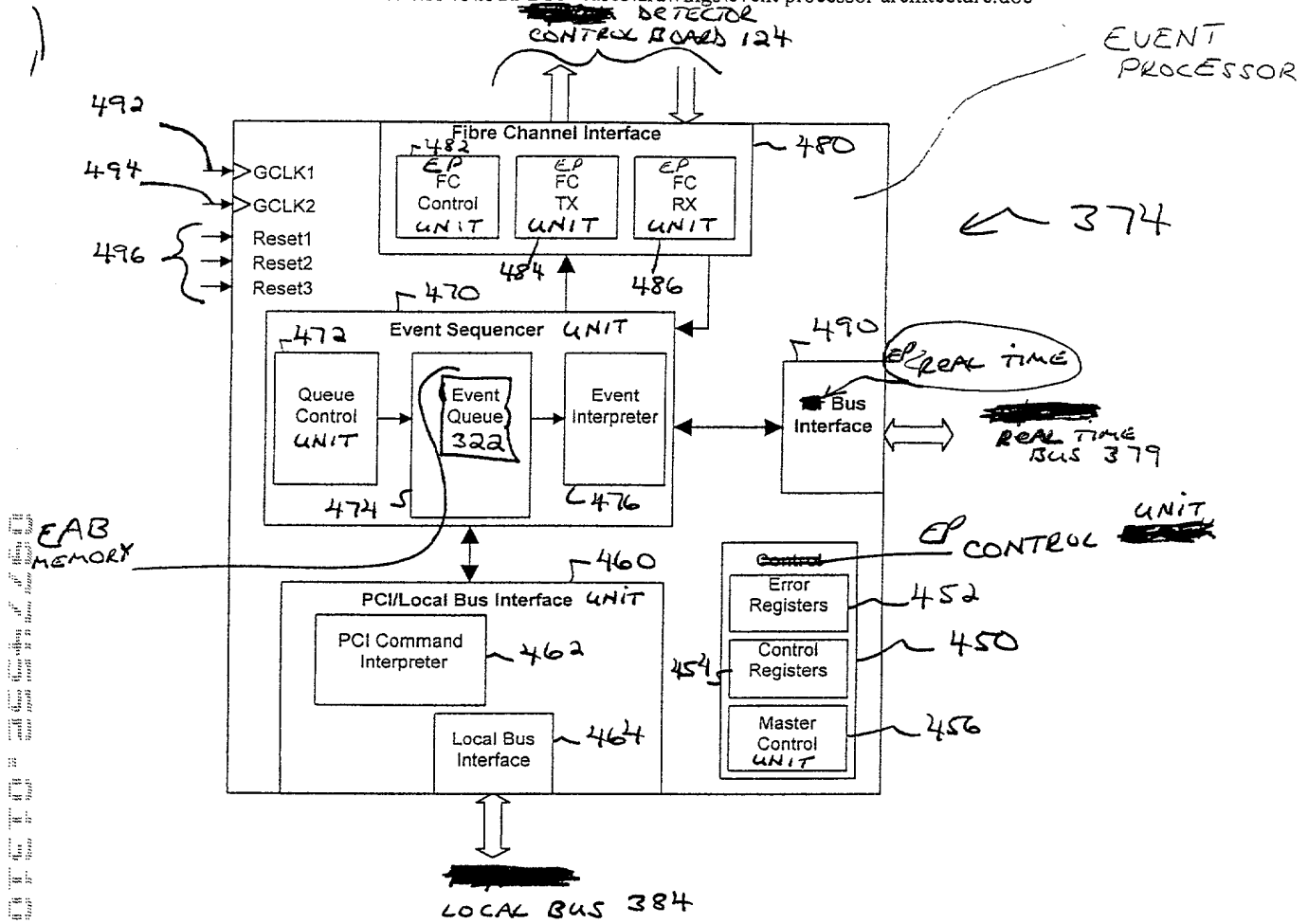


FIG. 25

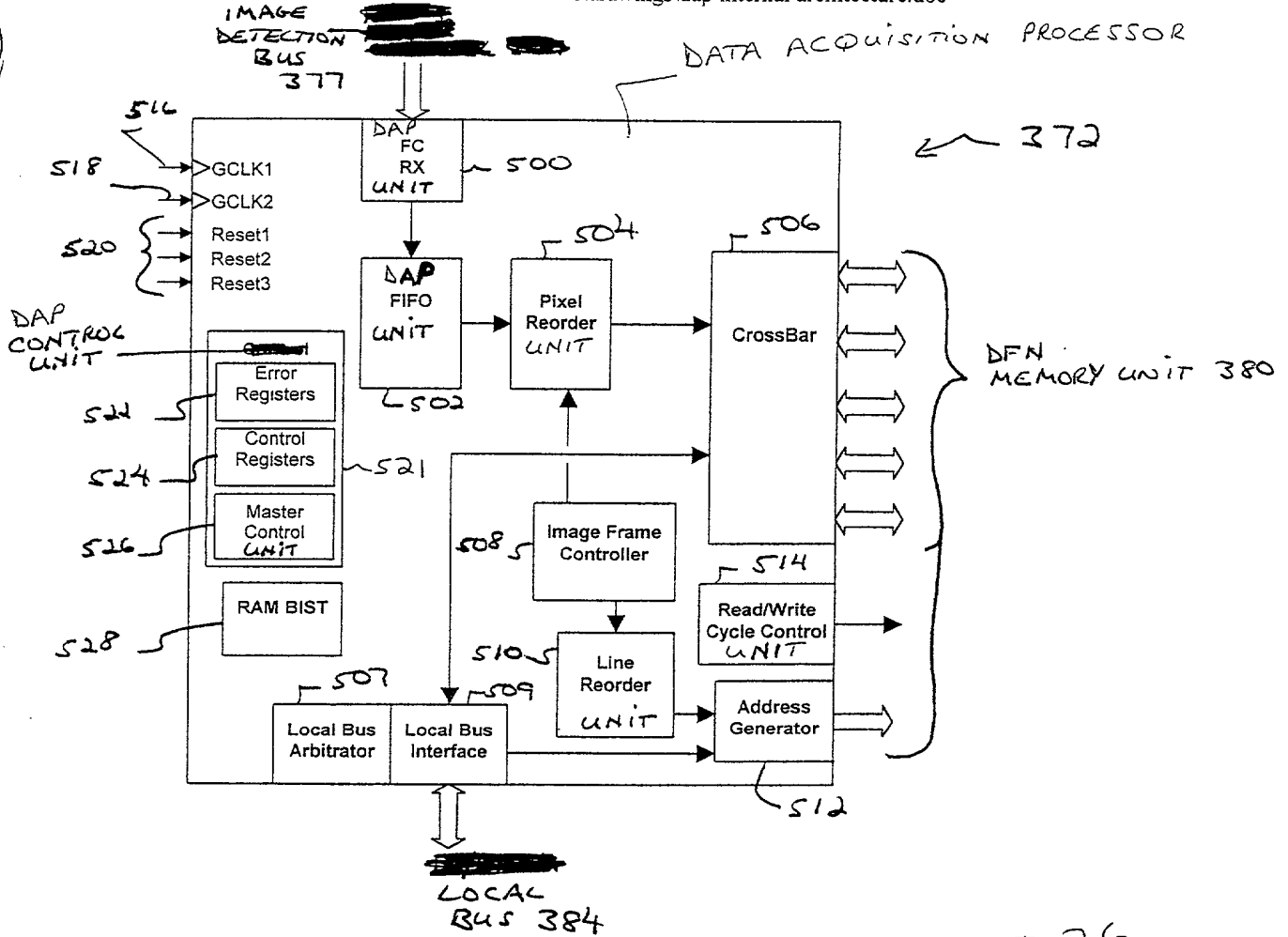


FIG. 26

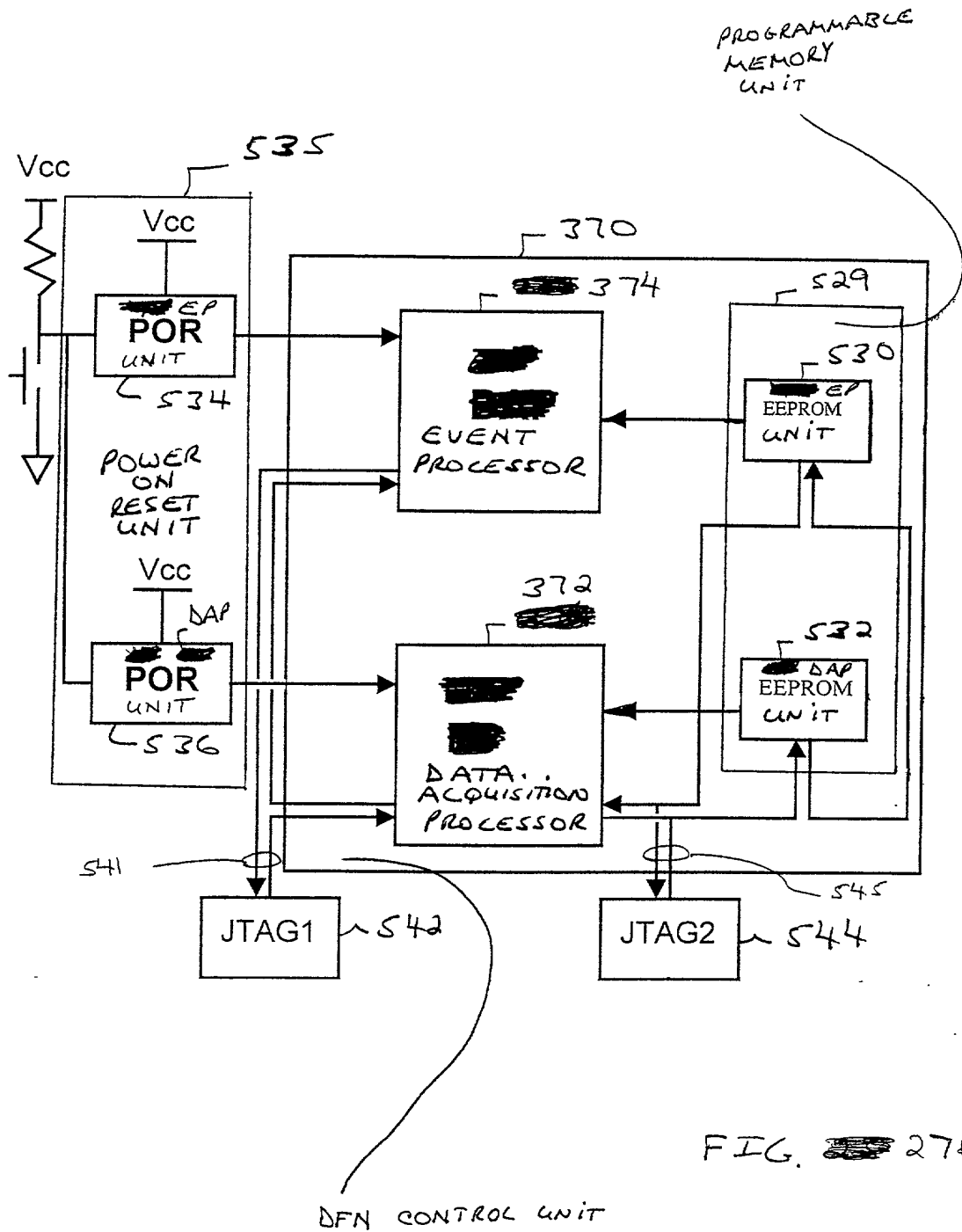
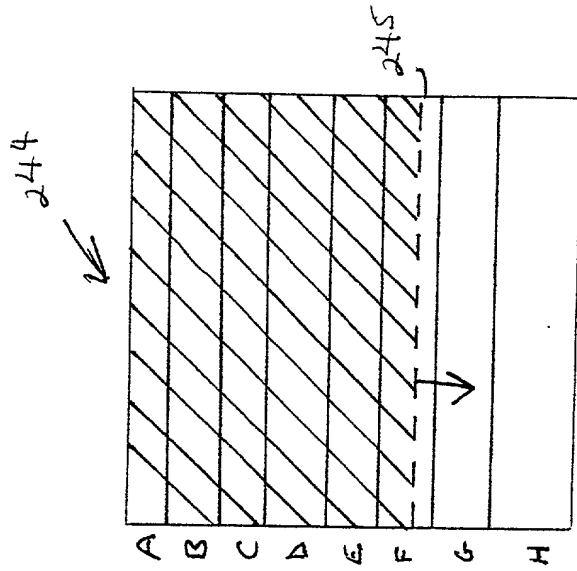
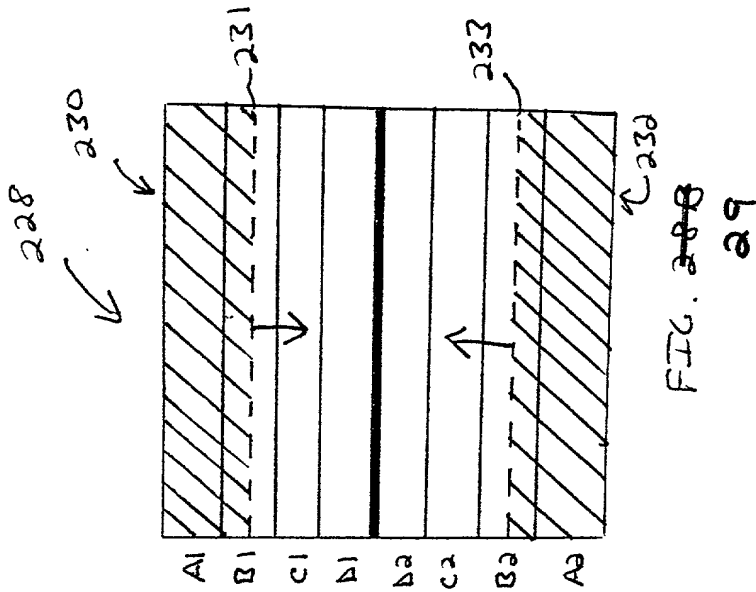
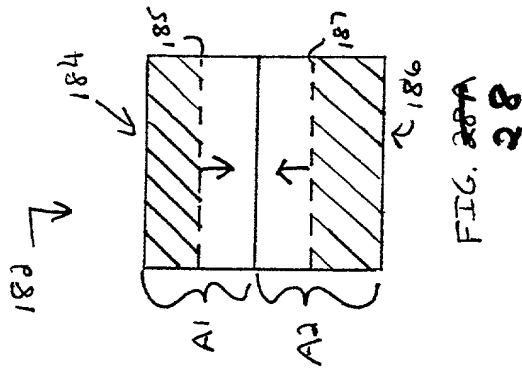


FIG. 27



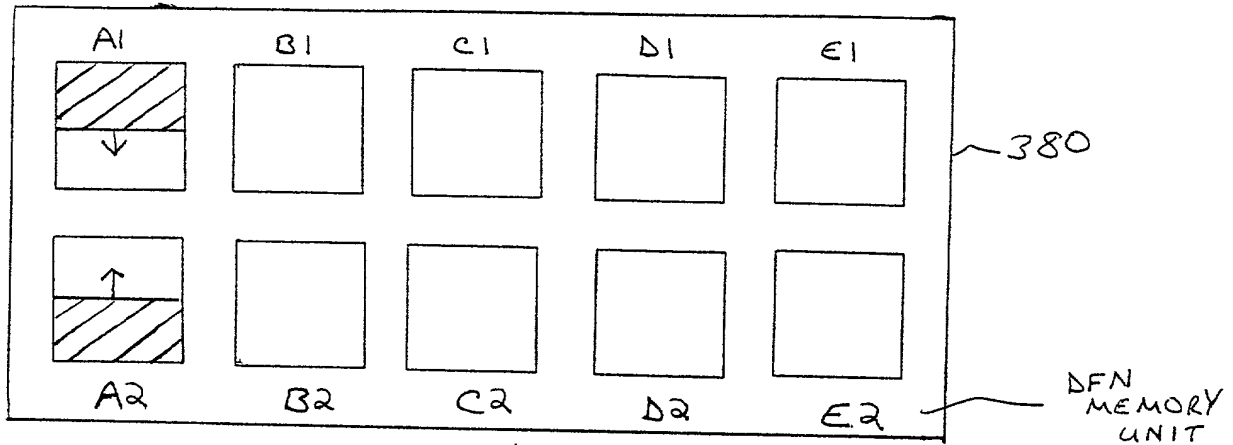


FIG. ~~31A~~ 31

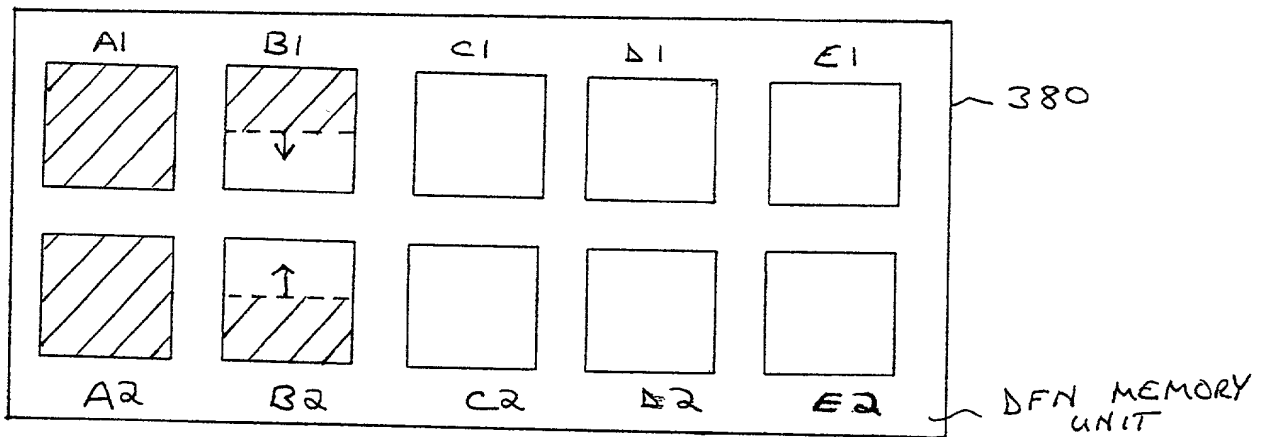


FIG. ~~31B~~ 32

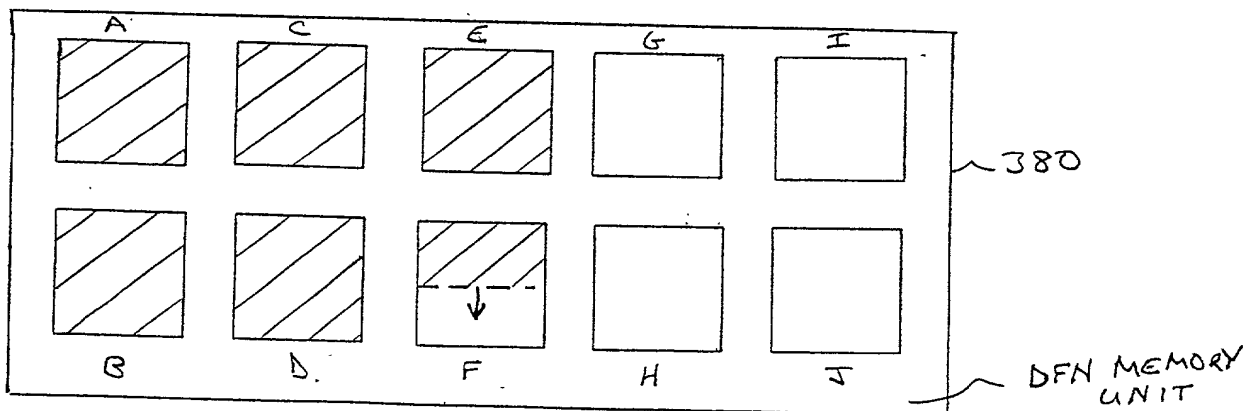


FIG. ~~32A~~ 33

334

A1
A2

FIG. ~~34A~~
34

334

A1
B1
C1
A1
A2
C2
B2
A2

FIG. ~~34B~~
35

334

A
B
C
A
E
F
G
H

FIG. ~~34C~~
36

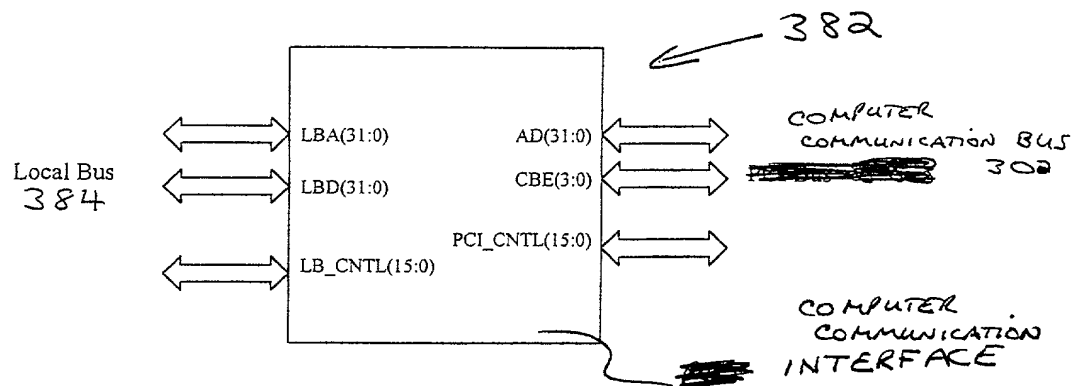


FIG. 37

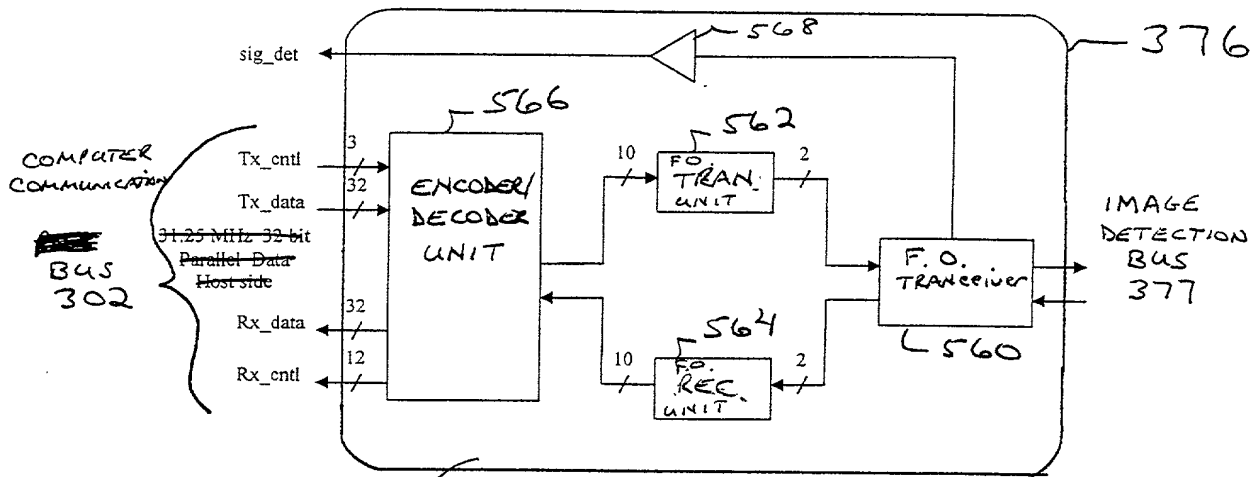


IMAGE DETECTION INTERFACE

FIG. 38

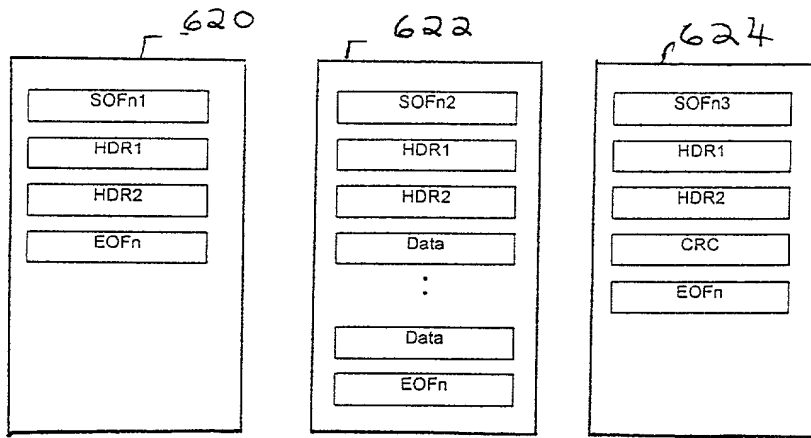


FIG. 39

FIG. 40

FIG. 41

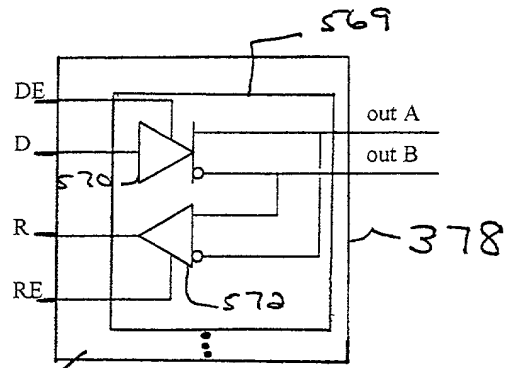


FIG. 42

REAL TIME
BUS INTERFACE

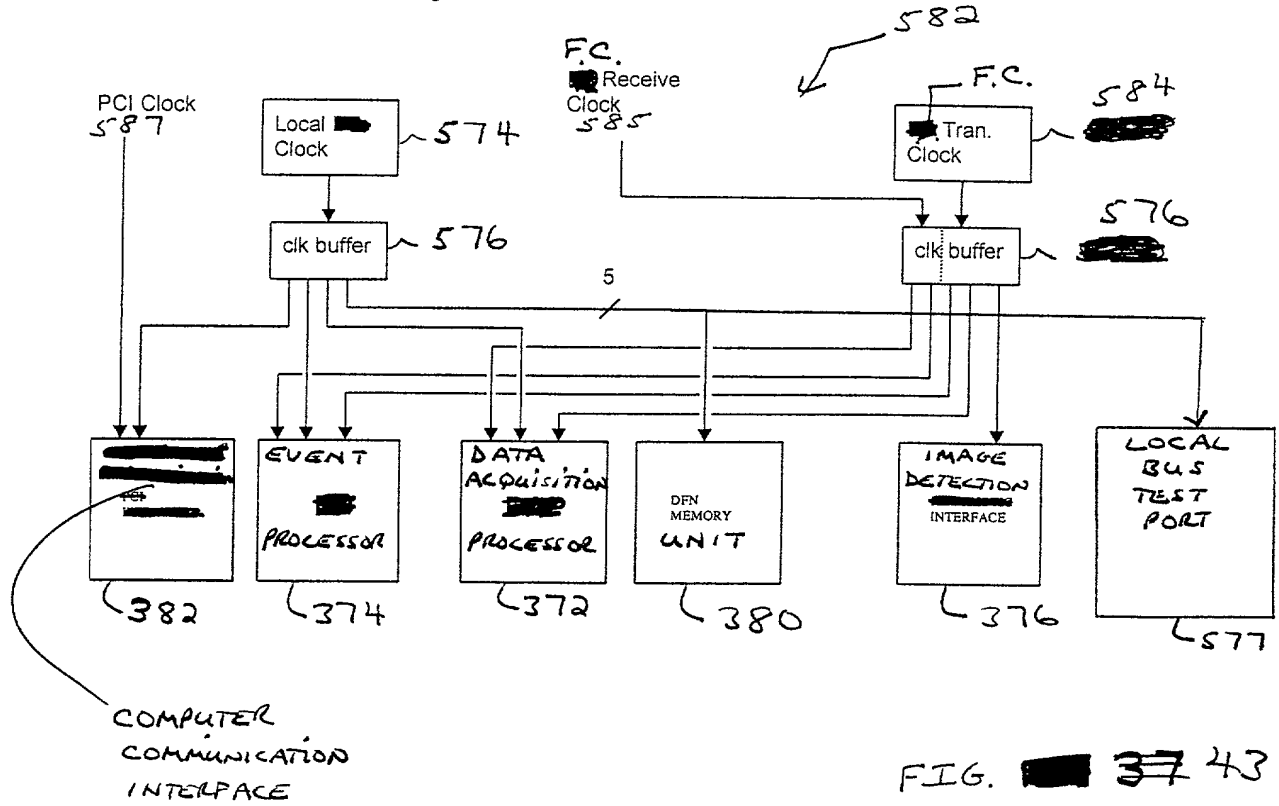


FIG. 37 43

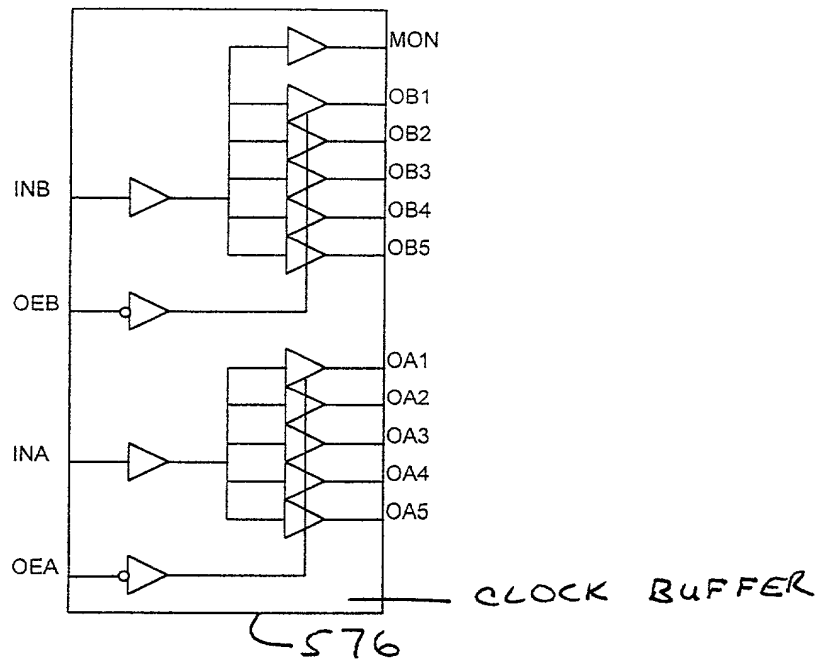


FIG. ~~44~~ 44

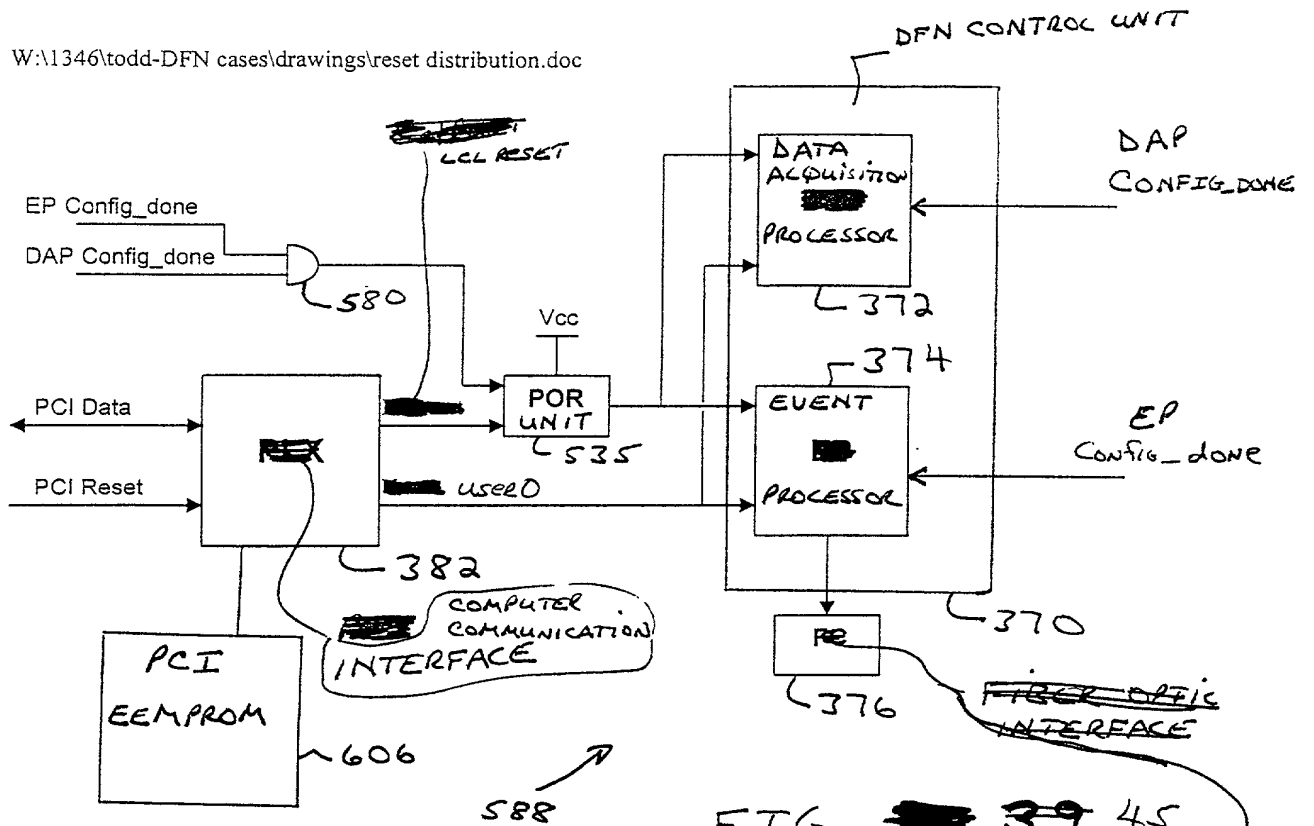


FIG. ~~39~~ 45

IMAGE DETECTION INTERFACE ~~COMPUTER COMMUNICATION INTERFACE~~

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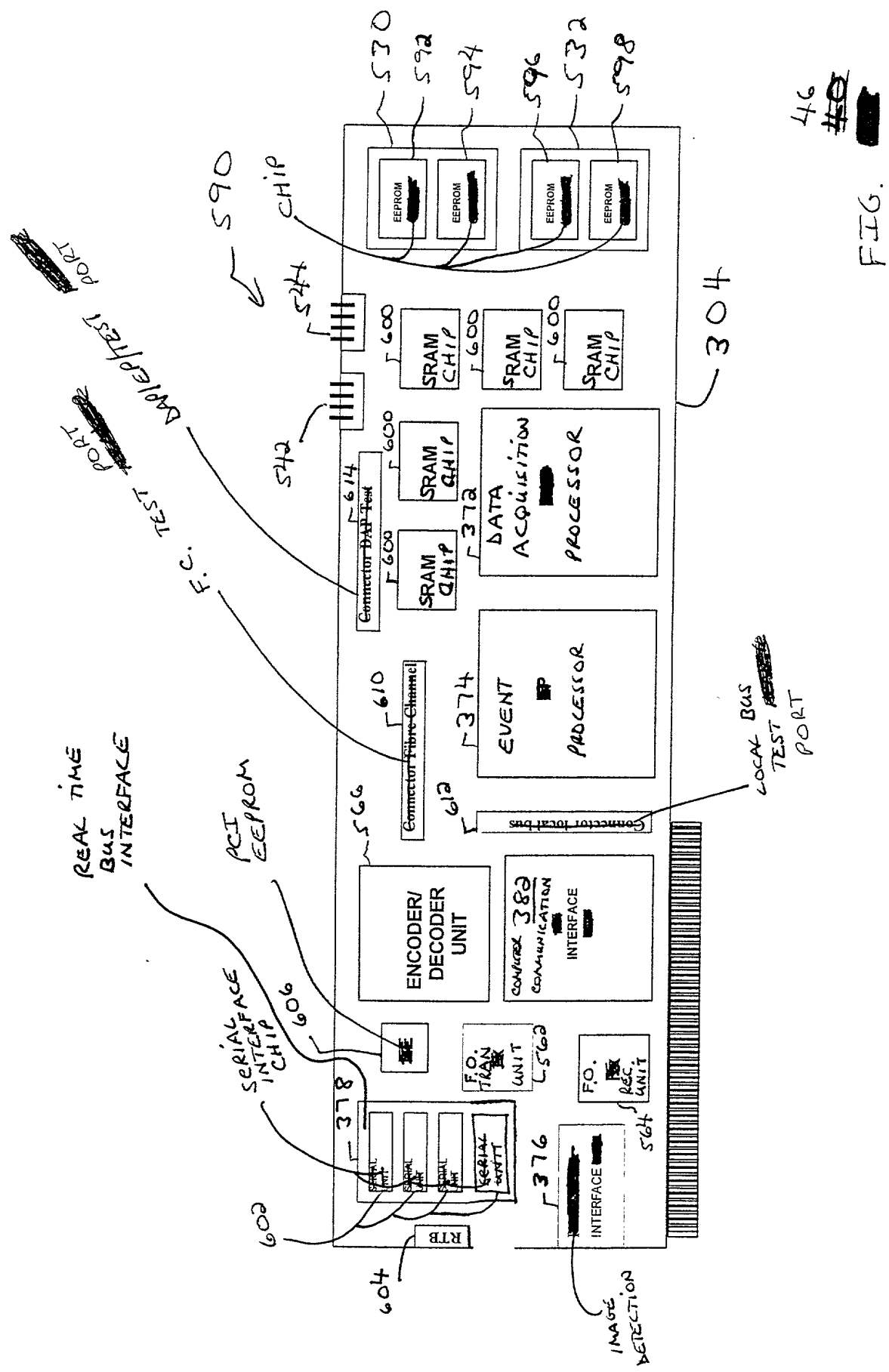
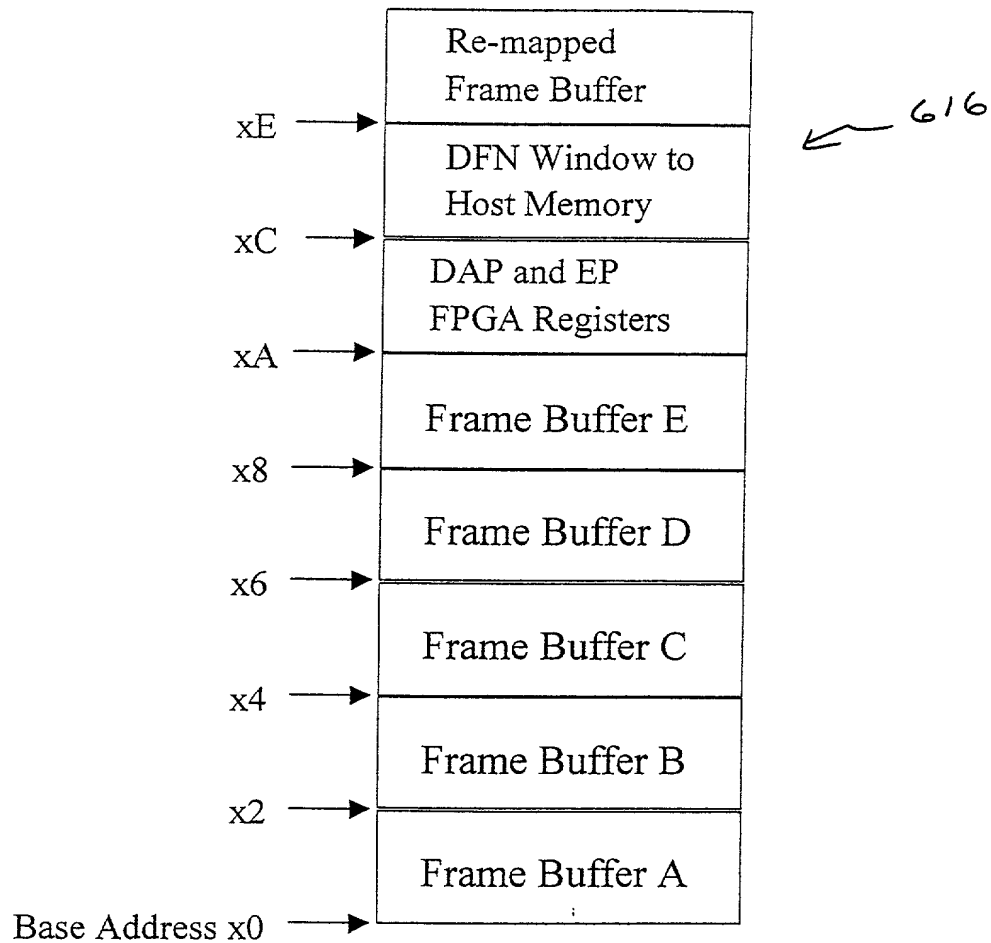


FIG.

46
#0



Mapping of 16 MByte PCI Address Space

FIG. ~~41~~ 47

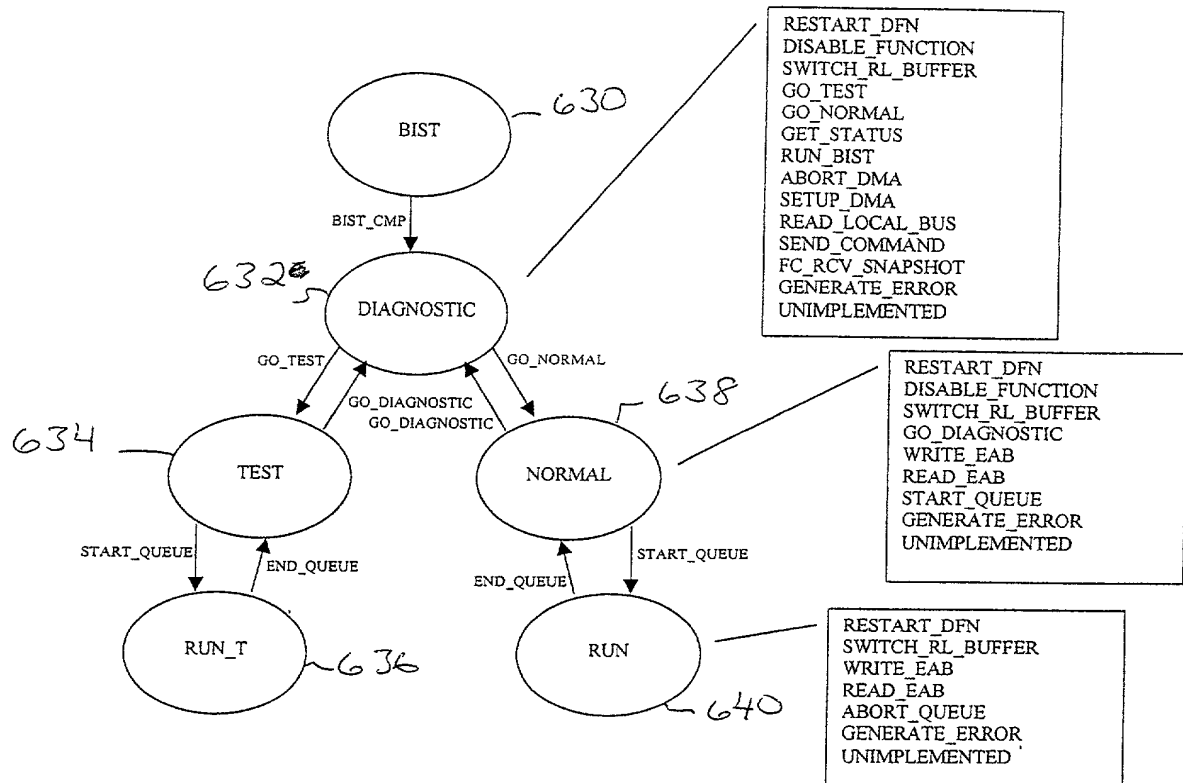


FIG. 48

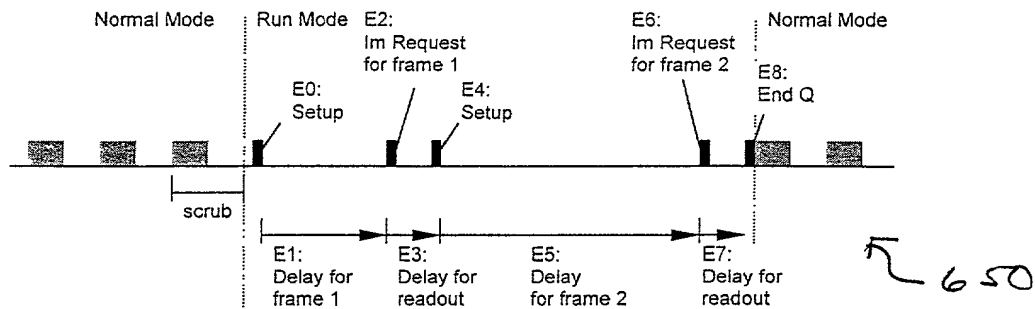


FIG. 49

Event Mnemonic	Event (showing size of arguments)	Op Code (hex)	Data (bytes)	Total (bytes)
Endq	Endq	14	0	1
Delay (T)	Delay (0xff ff ff ff)	10	4	5
Send (command, value)	Send (0xff ff ff ff, 0xff ff ff ff)	04	8	9
LoopKN (K, N)	LoopKN (0xff ff, 0xff)	0C	3	4
LoopKF (K, F)	LoopKF (0xff ff, 0xff ff ff)	0D	5	6
Wait (F)	Wait (0xff ff ff)	09	3	4
Flag (F)	Flag (0xff ff ff)	08	3	4

FIG. 50

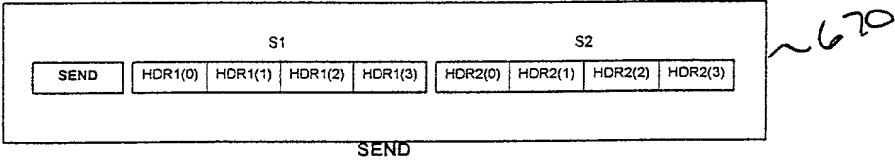


FIG. 51

Error Mnemonic	Description of Error
FC_TIMEOUT	Timeout expired with no ACK detected
FC_BAD_ACK	ACK did not match transmitted command
FC_EXTRA_ACK	Unexpected ACK received
FC_EXTRA_CMD	New Send event while waiting for ACK from previous Send
SIG_DET_N	No input signal power on Fibre Channel (cable disconnected?)
RX_ERROR	Fibre Channel receiver detected bad data (defective chipset?)
WRDSYCN	Fibre Channel Data link unsynchronized
CRXS(1)	Bad Received CRC detected (Fiber-optic cable problem?)
CRXS(3) and CRXS(2)	Bad order in link state machine (defective chipset?)

← 672

FIG. 52

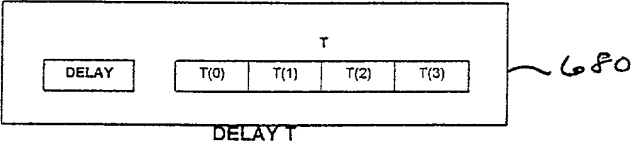


FIG. 53

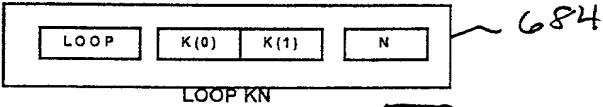
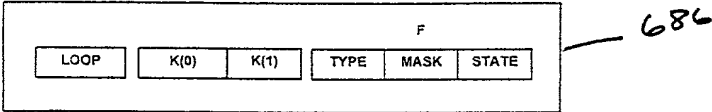
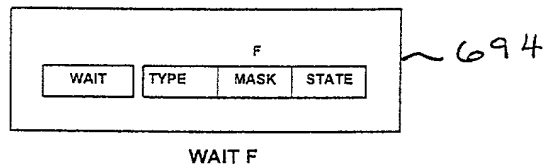


FIG. 54



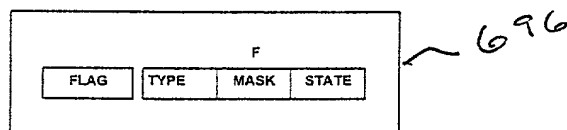
LOOP KF

FIG. 55



WAIT F

FIG. 56



FLAG F

FIG. 57



FIG. 58

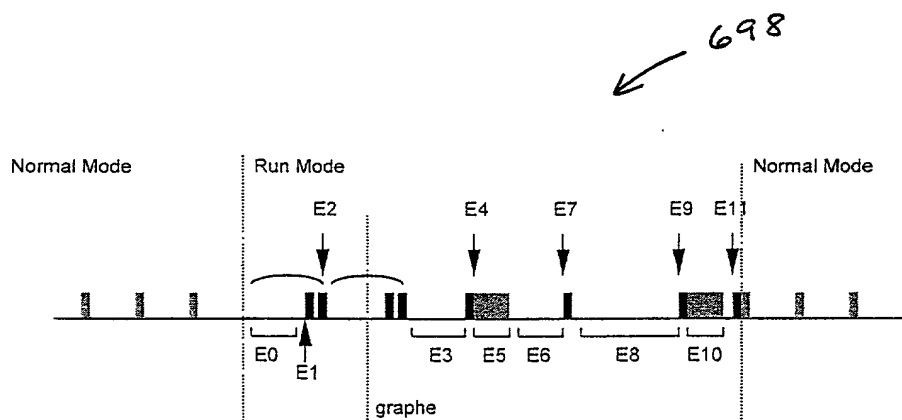


FIG. 59

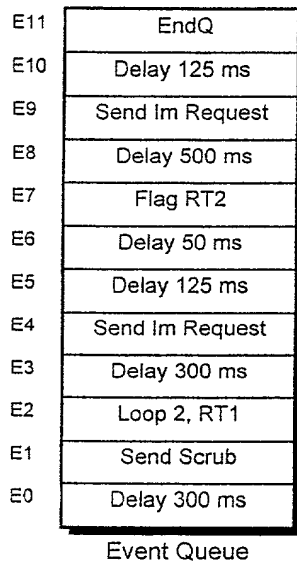


FIG. ~~60~~ 60

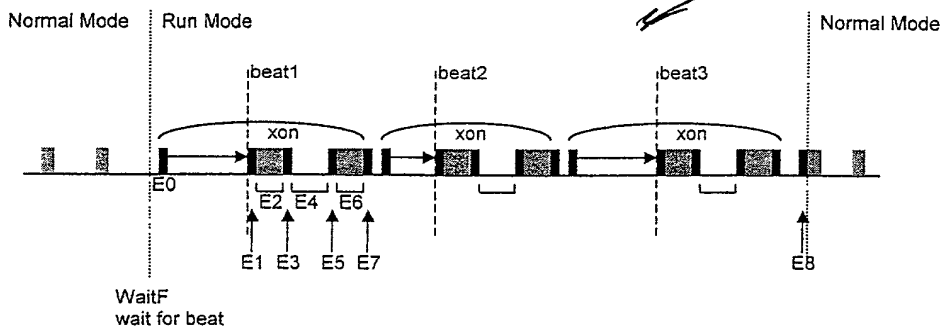
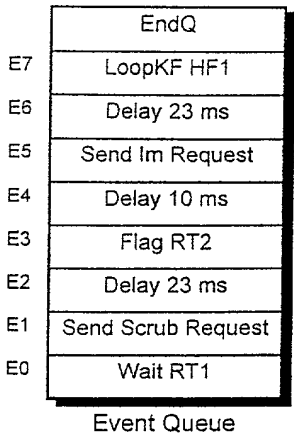


FIG. ~~61~~ 61



Event Queue

← 704

FIG. 62

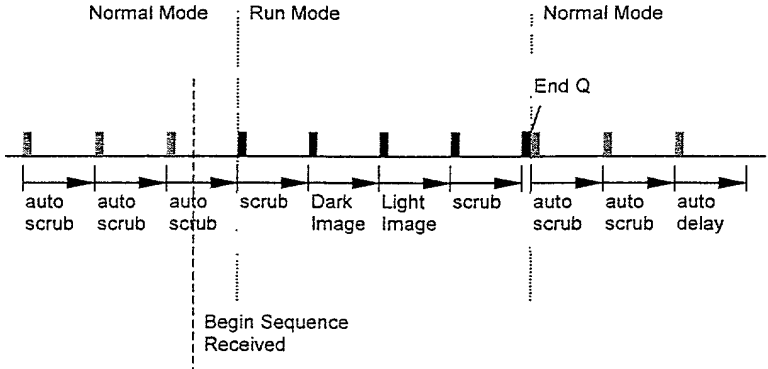


FIG. 63

```
sequence_begin ();

# define qv defaults:
%qv1 = ('delay_qv' => 5000);

# call frame with qv's
frame_typer1 (NULL, \%qv1, 1);

sequence_end ();
```

FIG. 64

```
sub frame
{
    $QVf = 'frame';

    %qv = ('delay_qv' => [10000]);
    %qp = ();

    compile_init(@_, \%qp, \%qv, $QVf);

    Delay('delay_qv');

    compile_finit();
}
```

FIG. 65

```
pDFN->DFNChangeQueueVariable
(
    (char *)SymName,      // variable name
    (char *)sndBuf,      // new value
    BufSize,              // num bytes to write
    (ULONG *)&debug      // developer info
);
```

FIG. 66

User Application

```
// load and run the event sequence
pDFN->DFNBeginSequenceNoMappingNoLog
(snum, "d:\\HF.bin");

//assign data to be passed
sndBuf = 25000;

// change the queue variable
pDFN->DFNChangeQueueVariable
(
    (char *)SymName,      // variable name
    (char *)sndBuf,      // new value
    (ULONG)sizeof sndBuf, // num bytes to write
    (ULONG *)&debug      // developer info
);
```

FIG. 67

Perl Script

```
sub frame_typer1
{
    $HFfrm = 'frame_typer1';

    %qv = ('delay_qv' => [20000]);
    %qp = ();

    $image_cmd = [0x800000, 0x0];

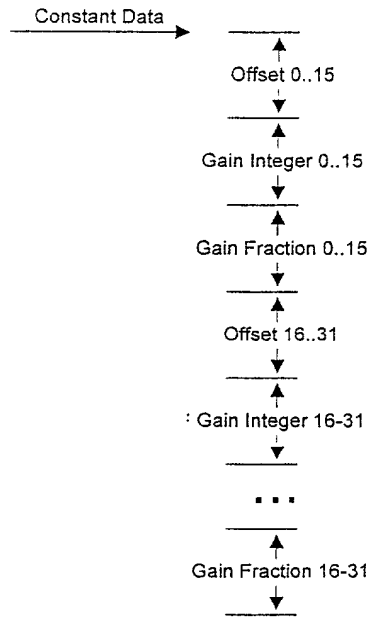
    compile_init(@_, \%qp, \%qv, $HFfrm);

    Send($image_cmd);
    Delay('delay_qv');
    LoopKF(2, 0xAAFF01);

    compile_finit();
}
```

FIG. 68

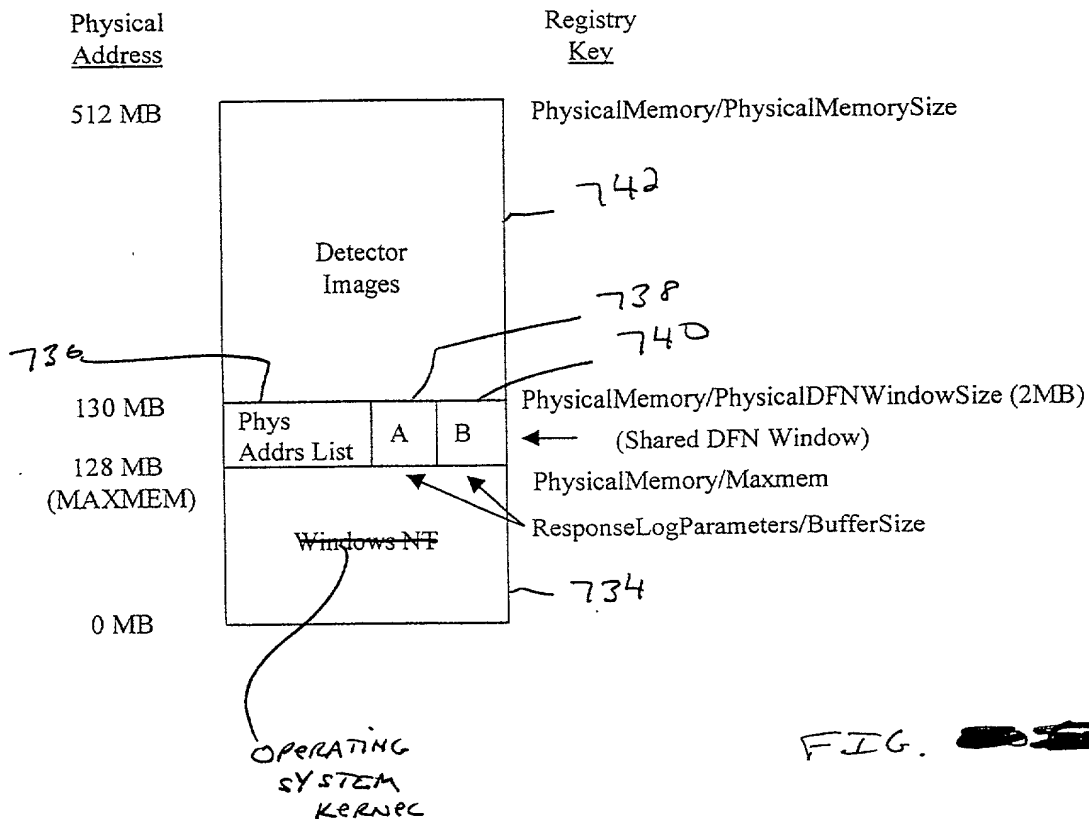
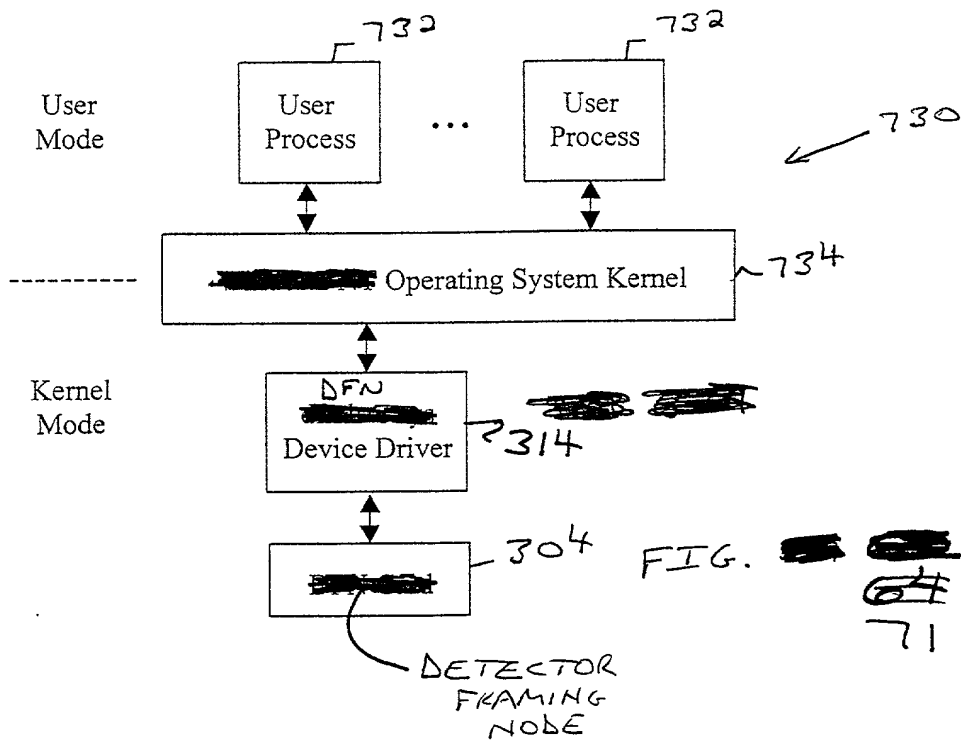
44



Constant Memory Format

FIG. ~~70~~
~~70~~
70

45



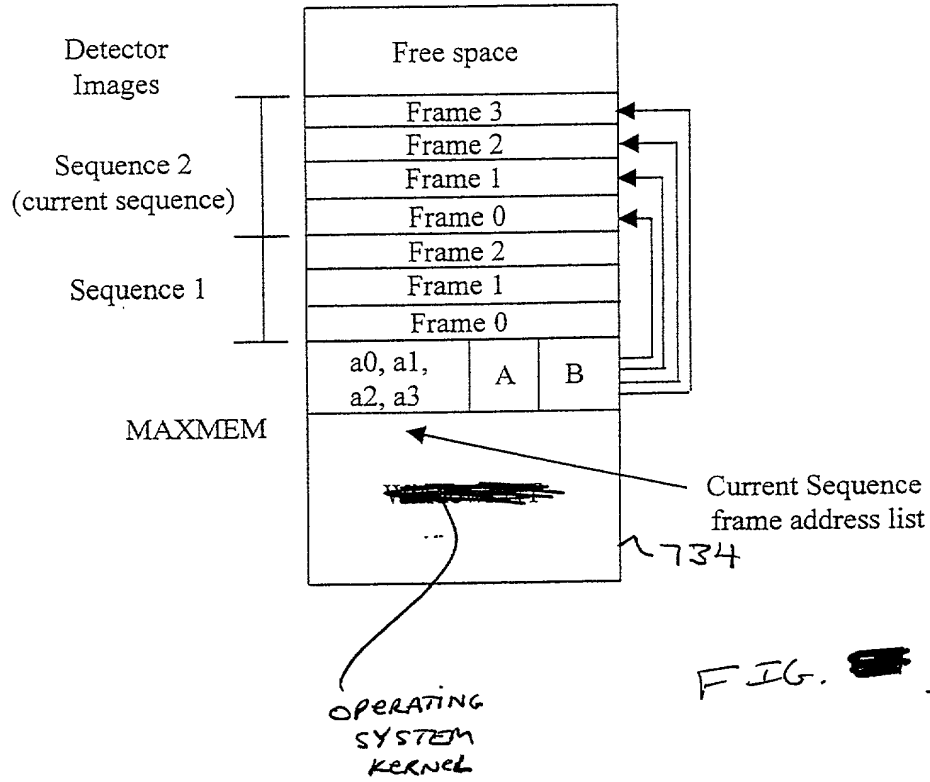


FIG. 73